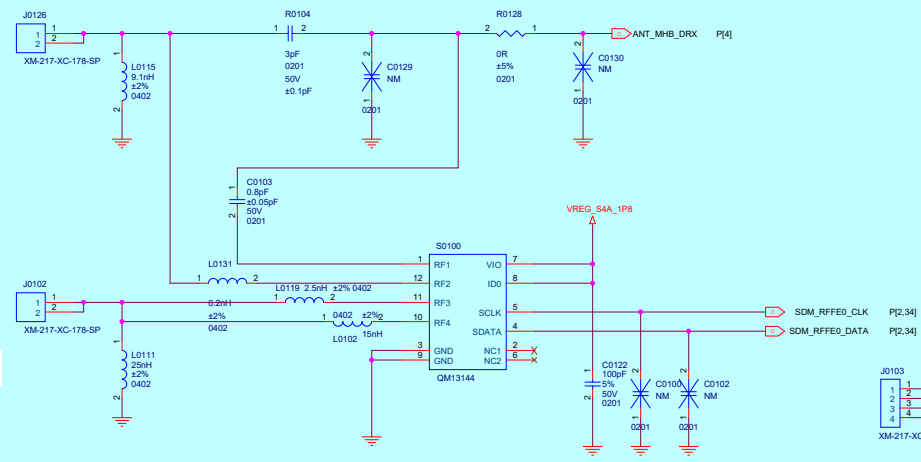
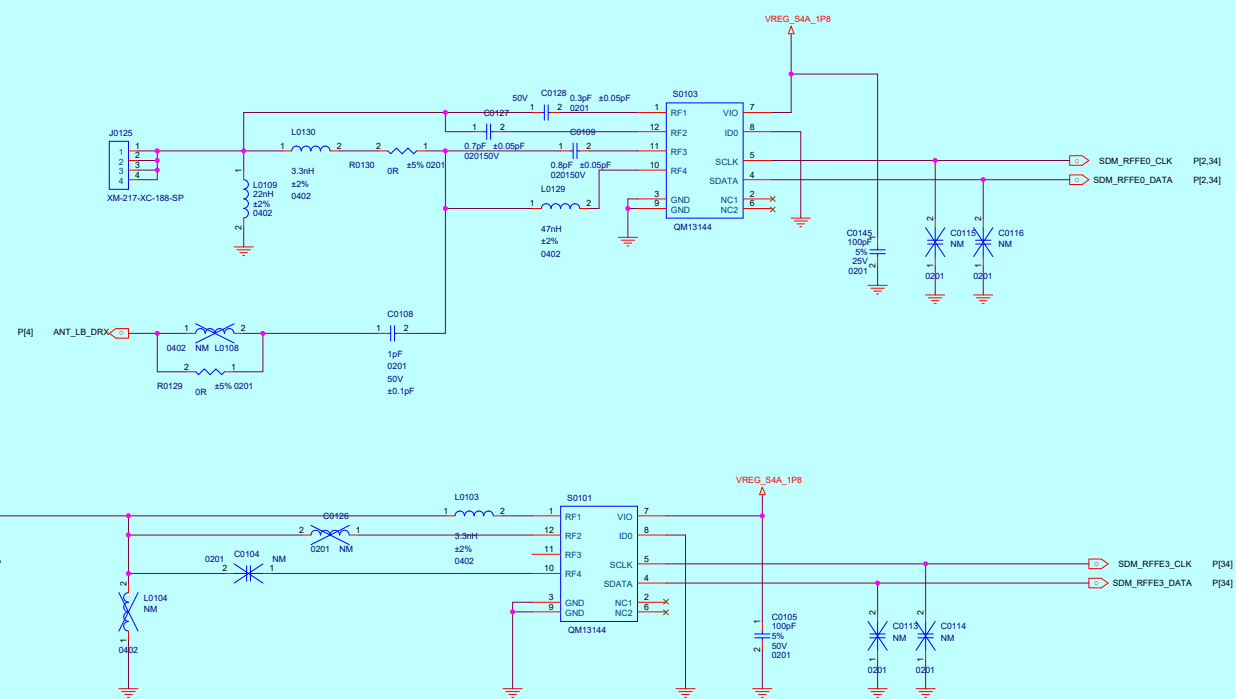


DRX_ANT_MHB



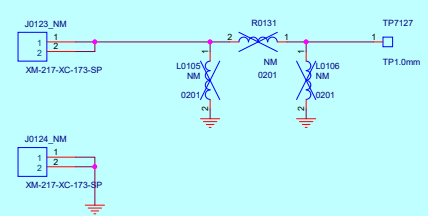
DRX_ANT_LB



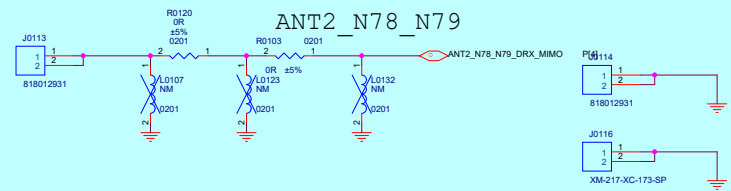
ANT11_B1 B34 DET+B3 MIMO



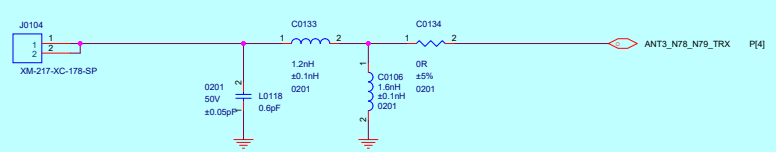
ANT12_B40 DETECT



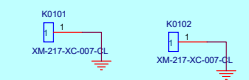
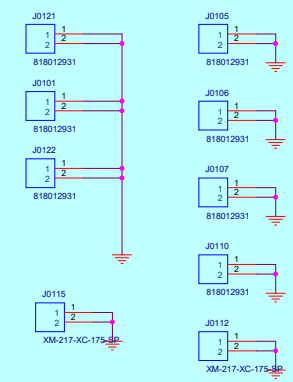
ANT2_N78_N79

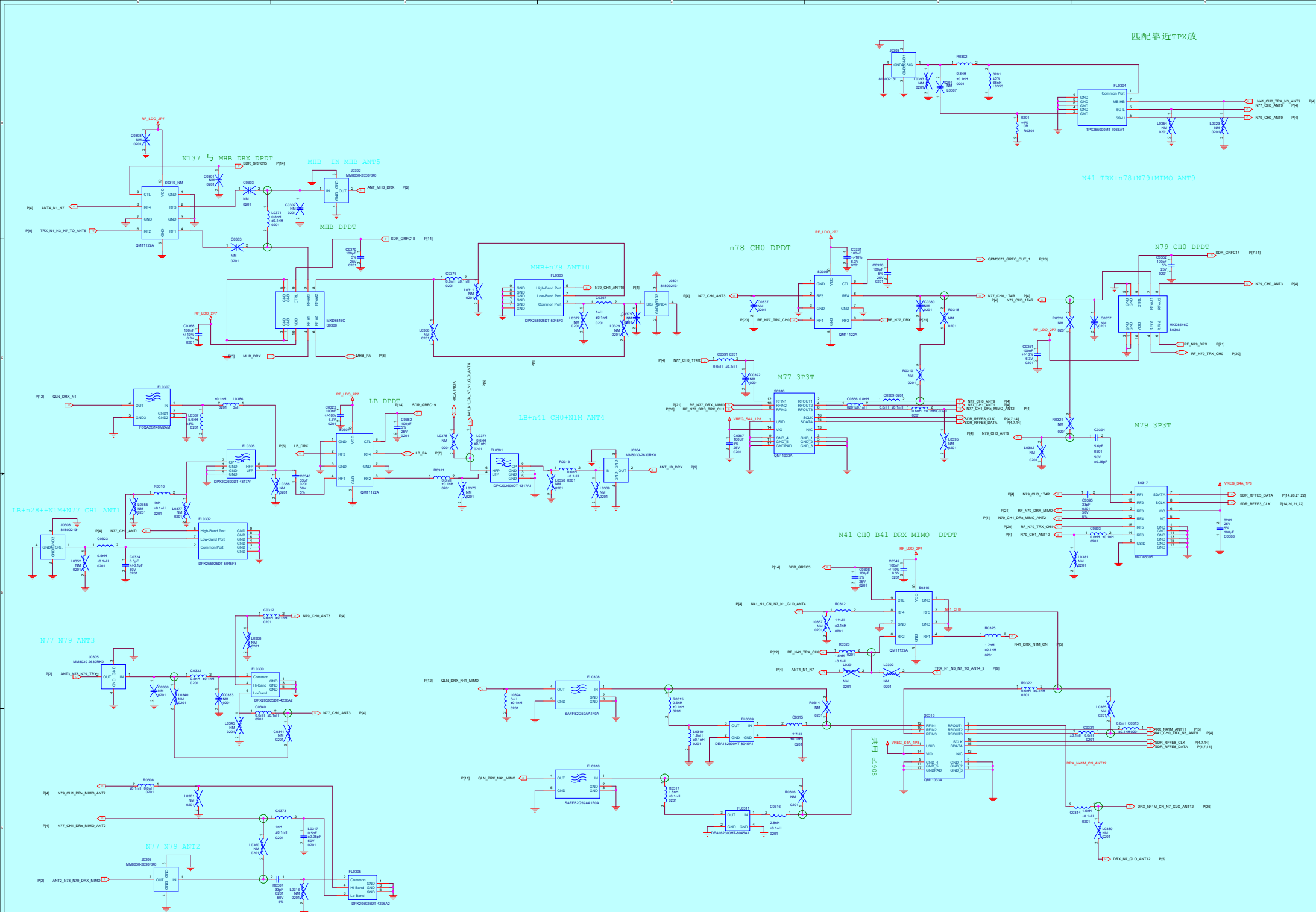


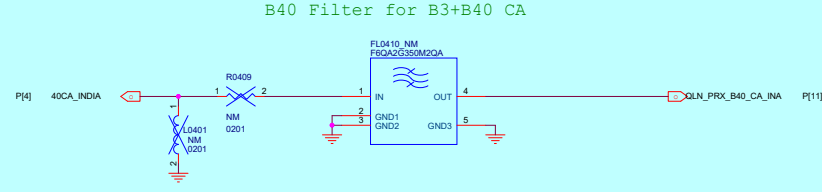
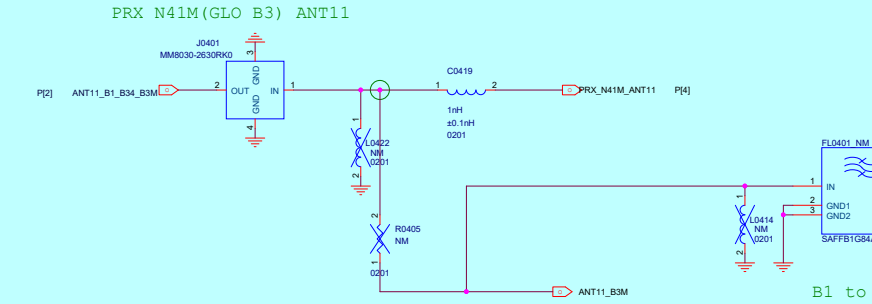
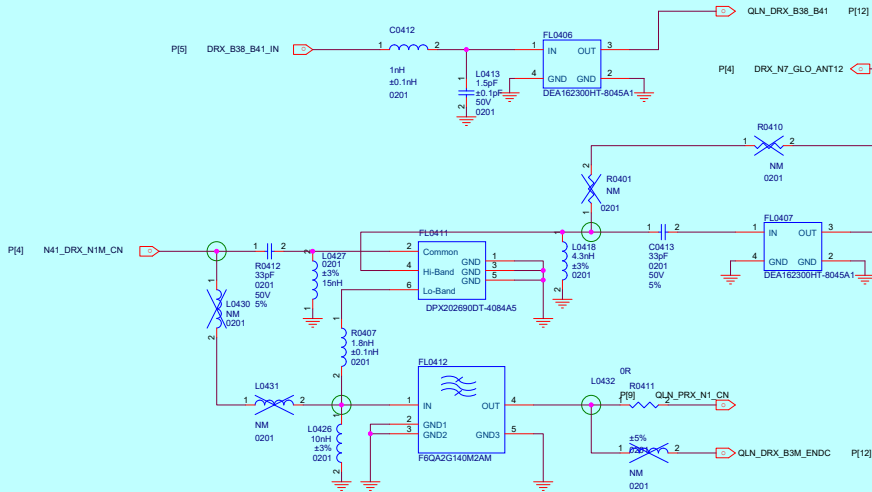
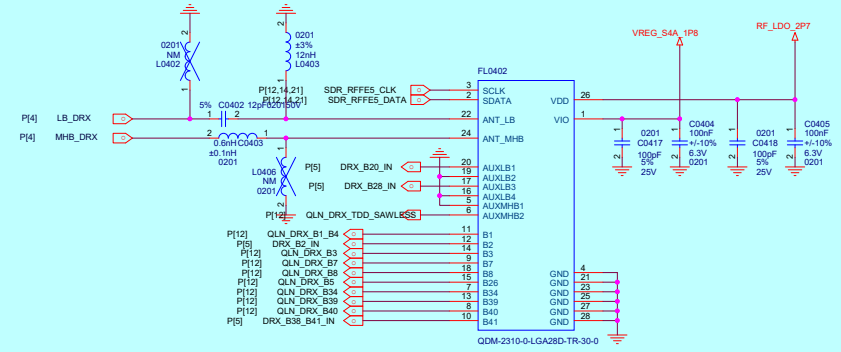
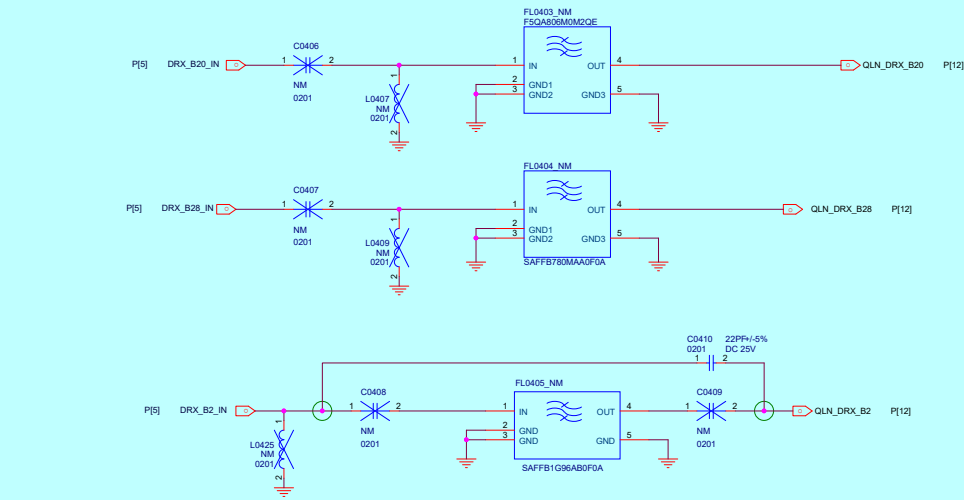
ANT3_N78_N79



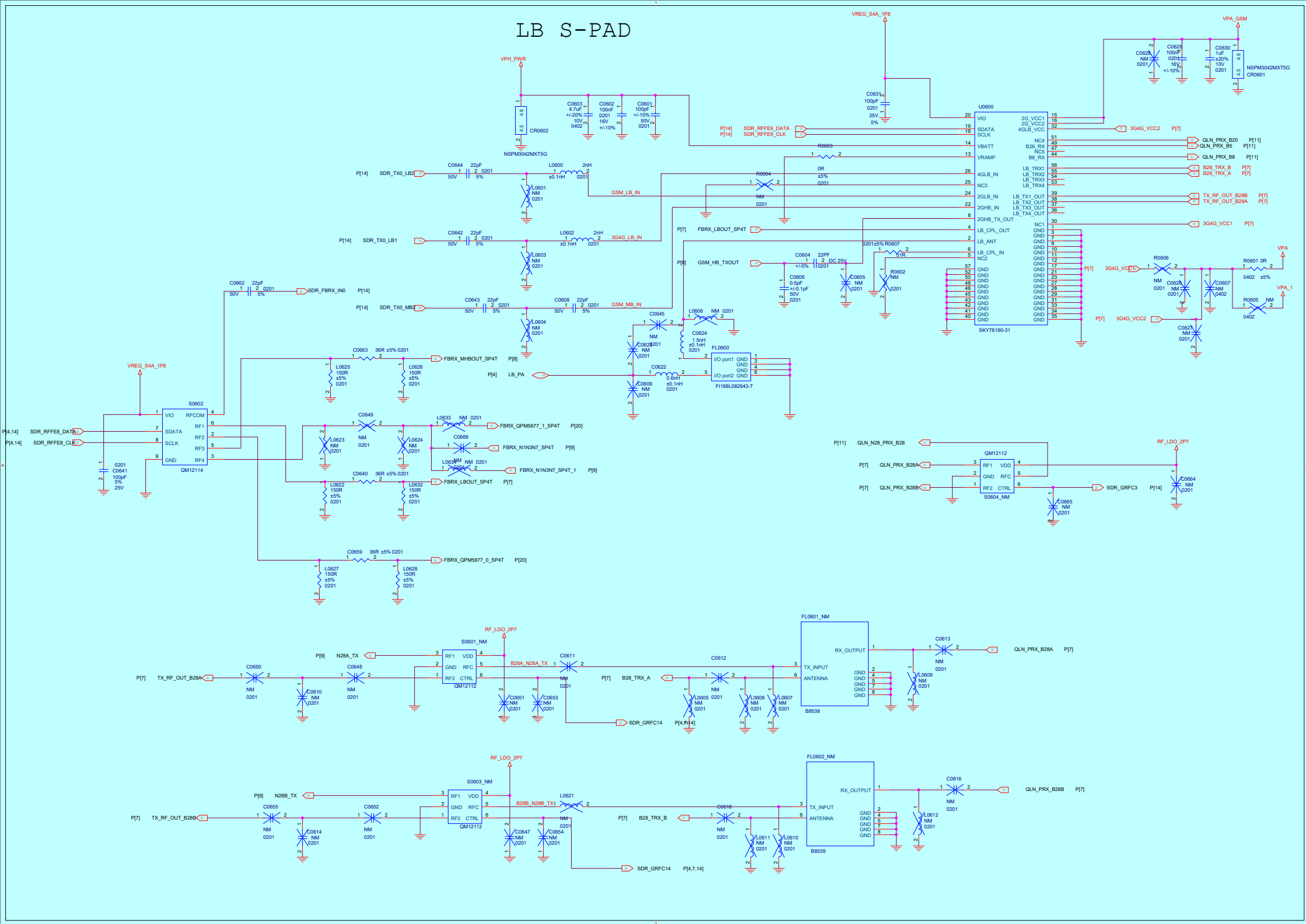
接地弹片



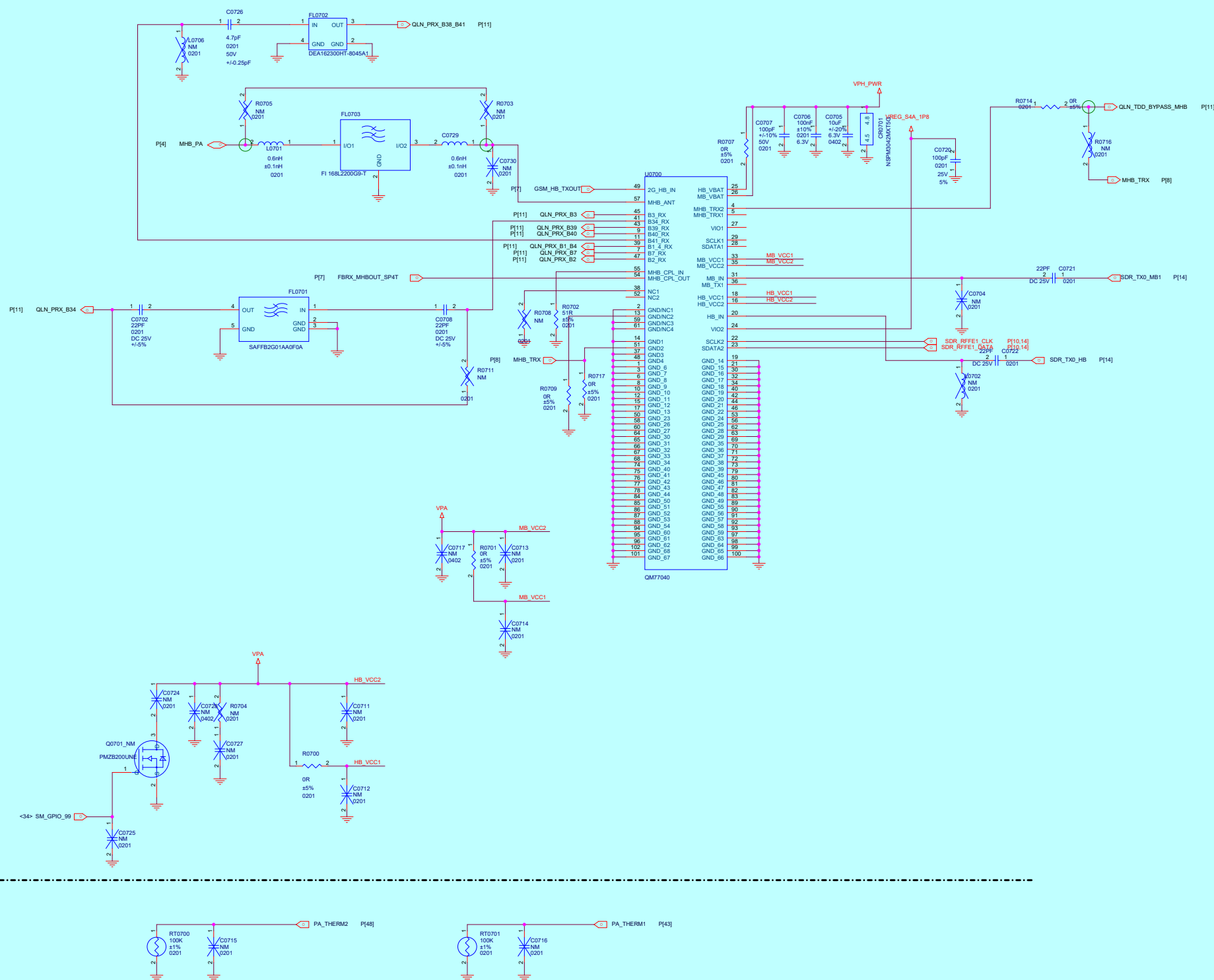




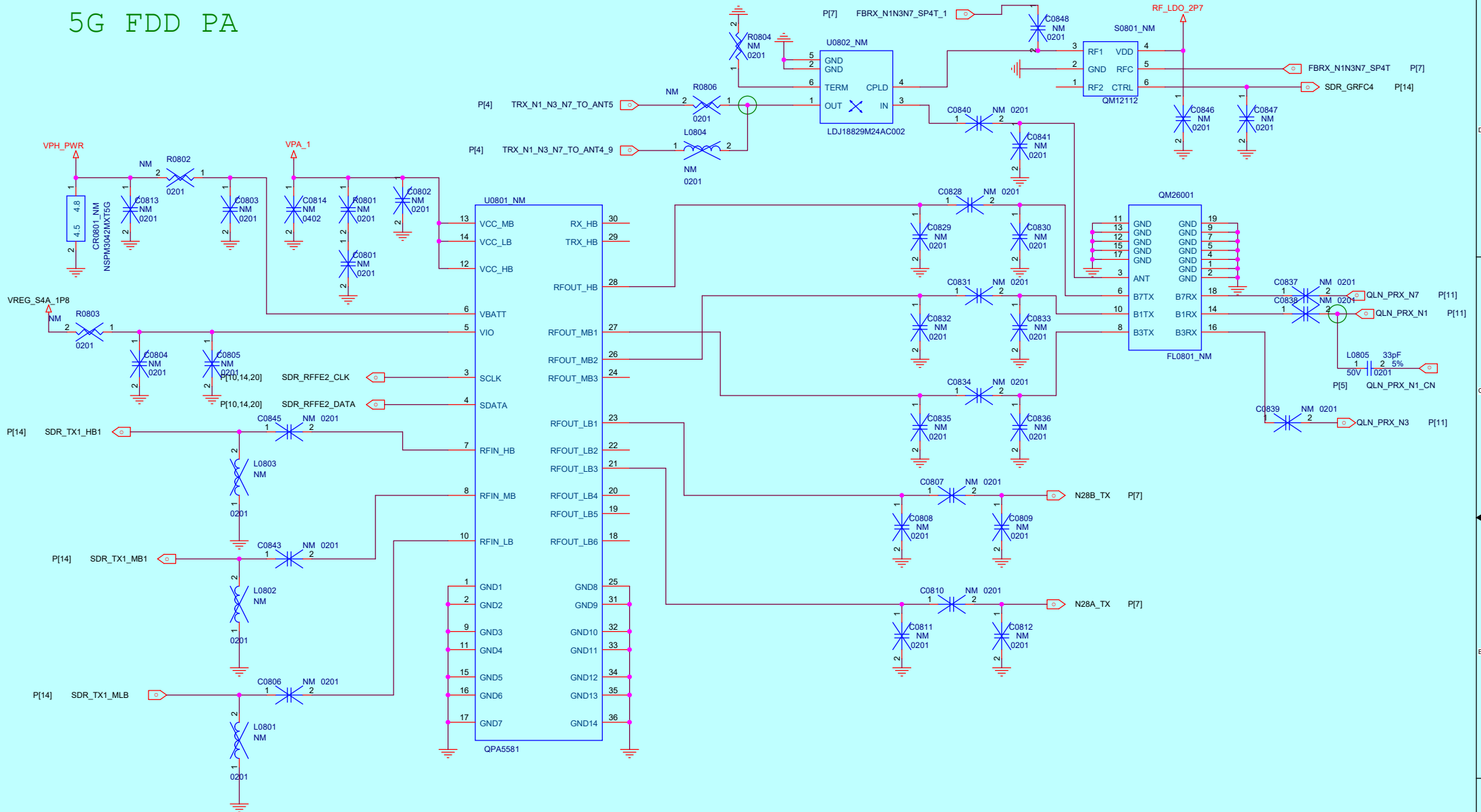
LB S-PAD



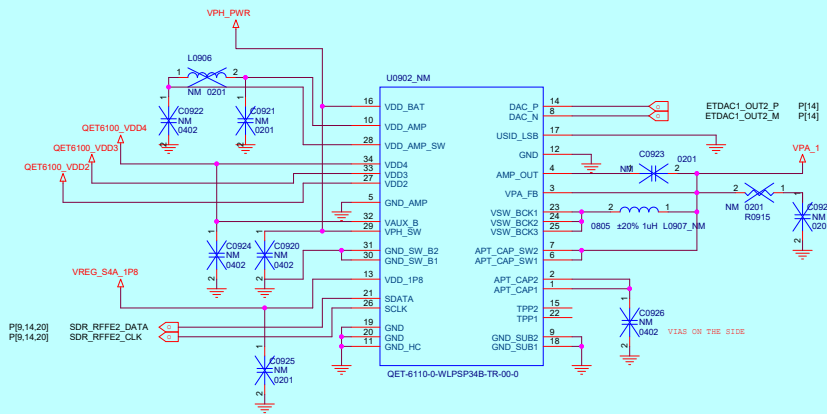
MHB S-PAD



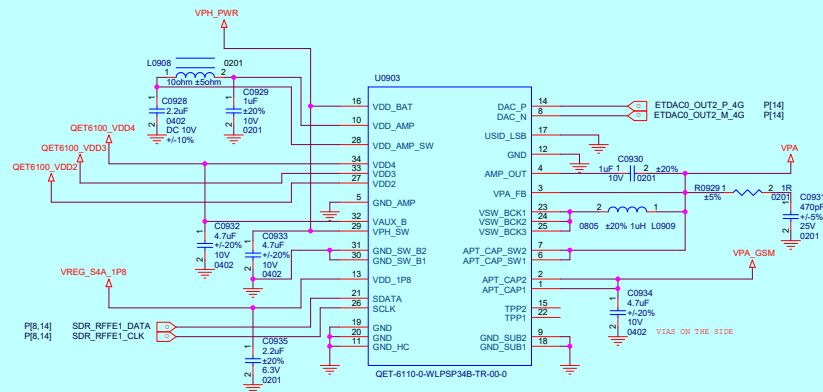
5G FDD PA

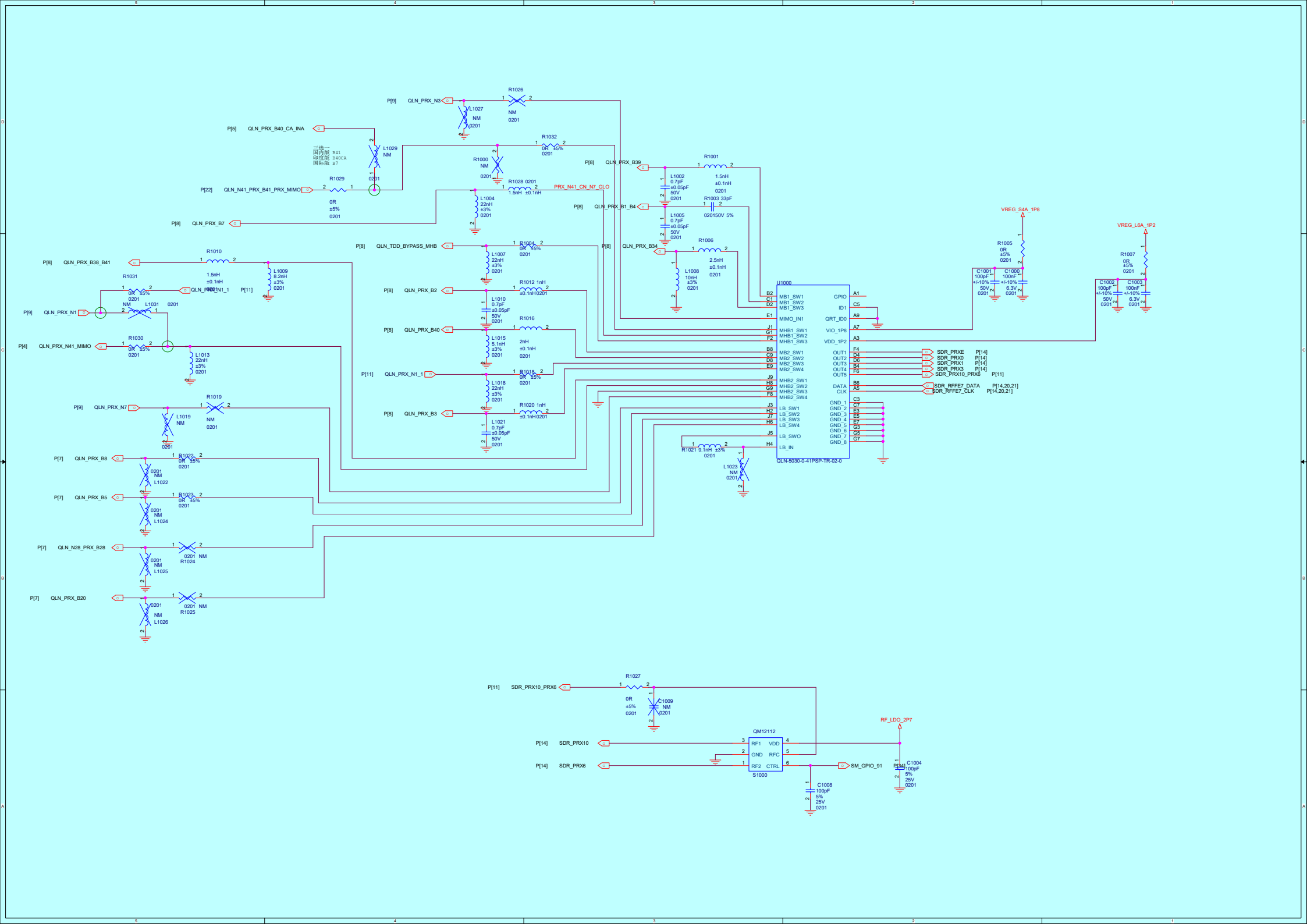


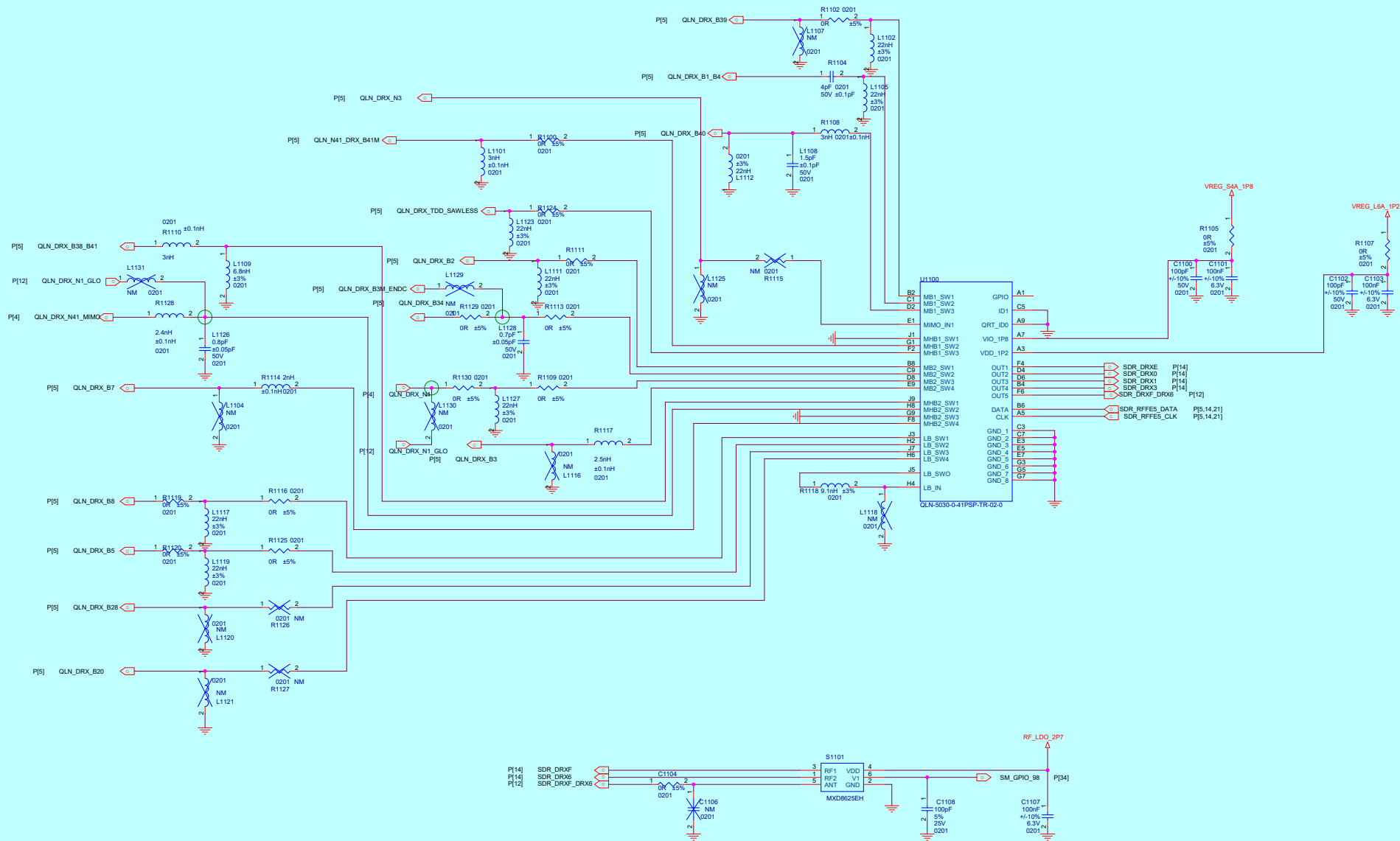
N28 QET

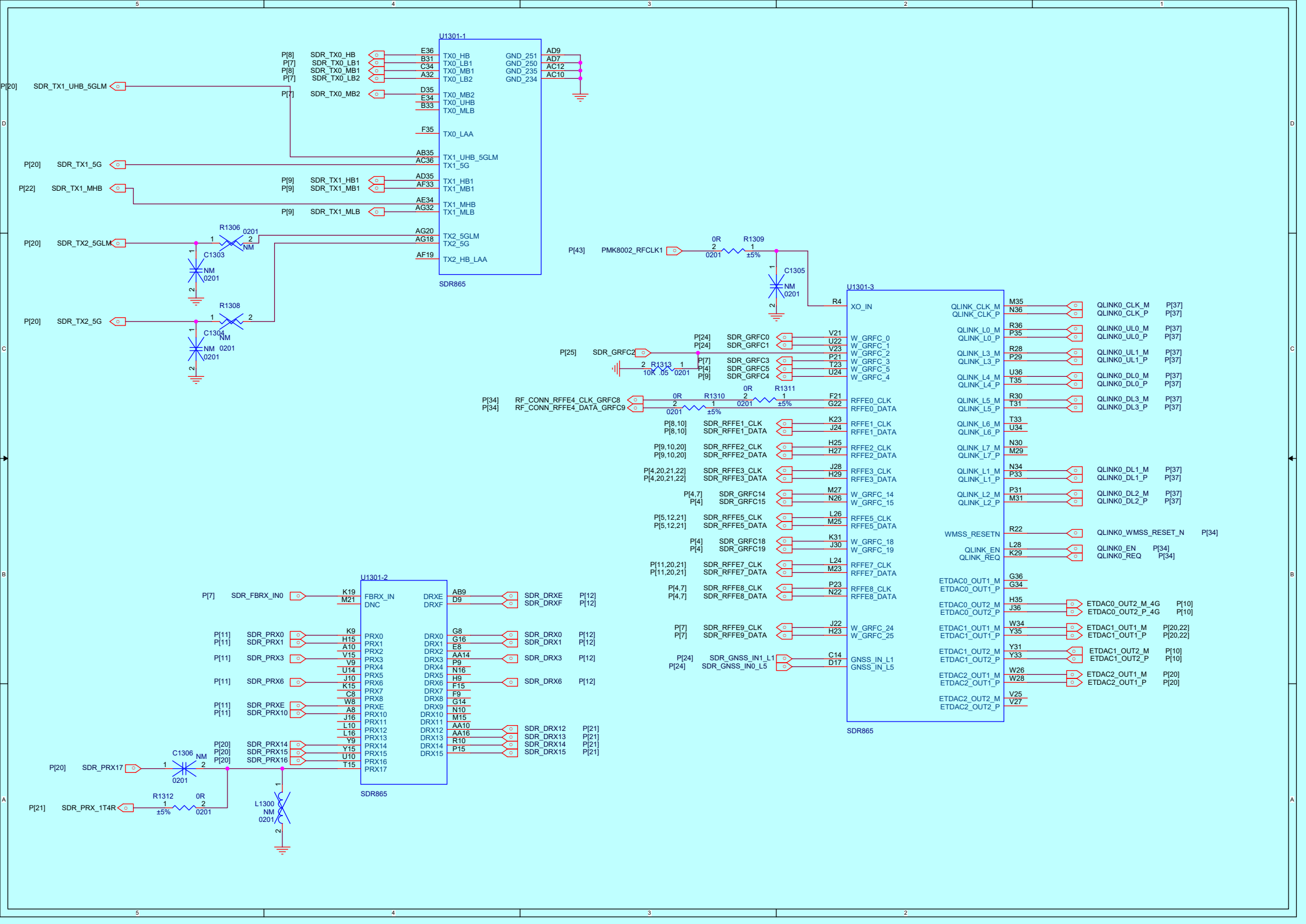


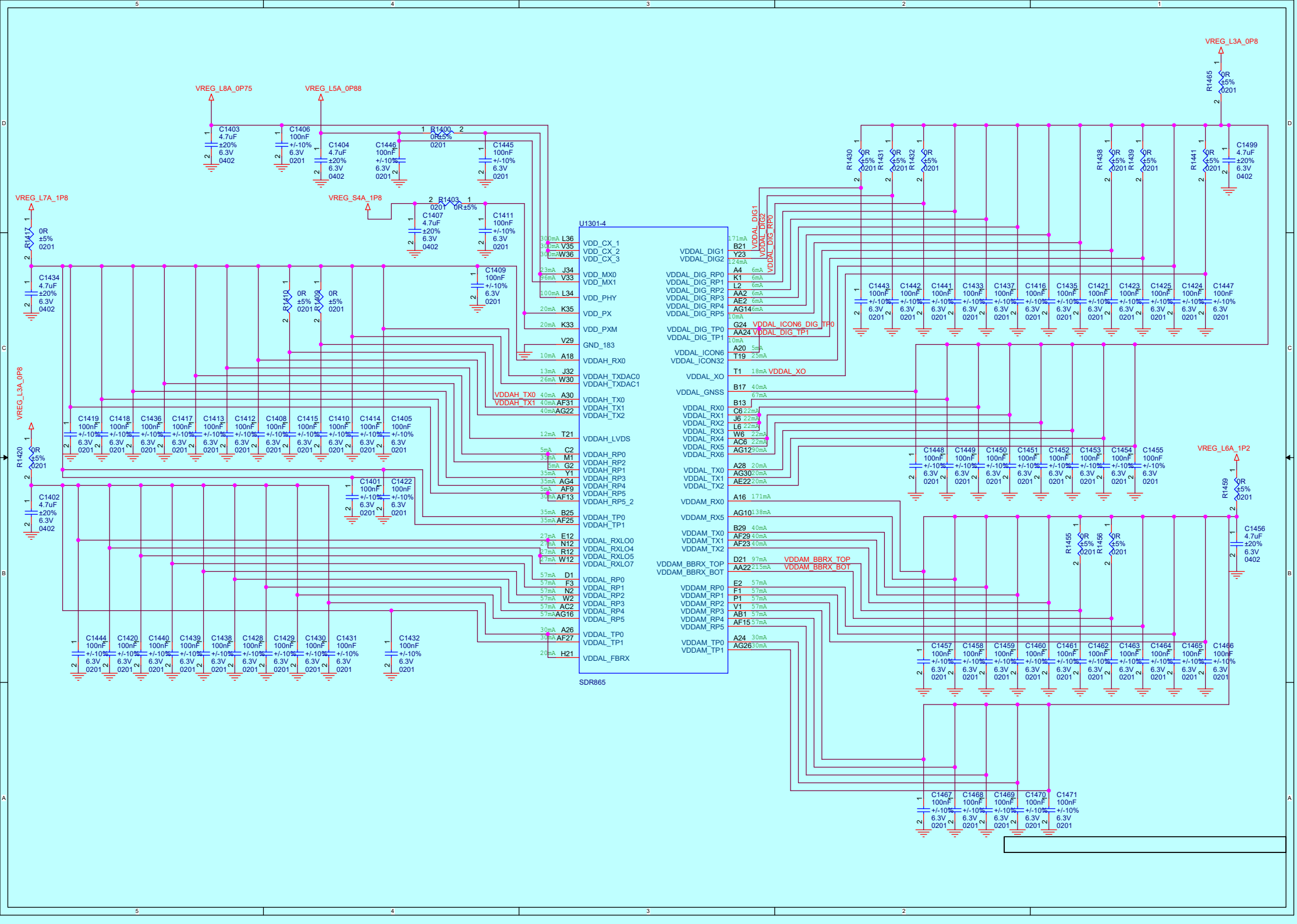
4G QET

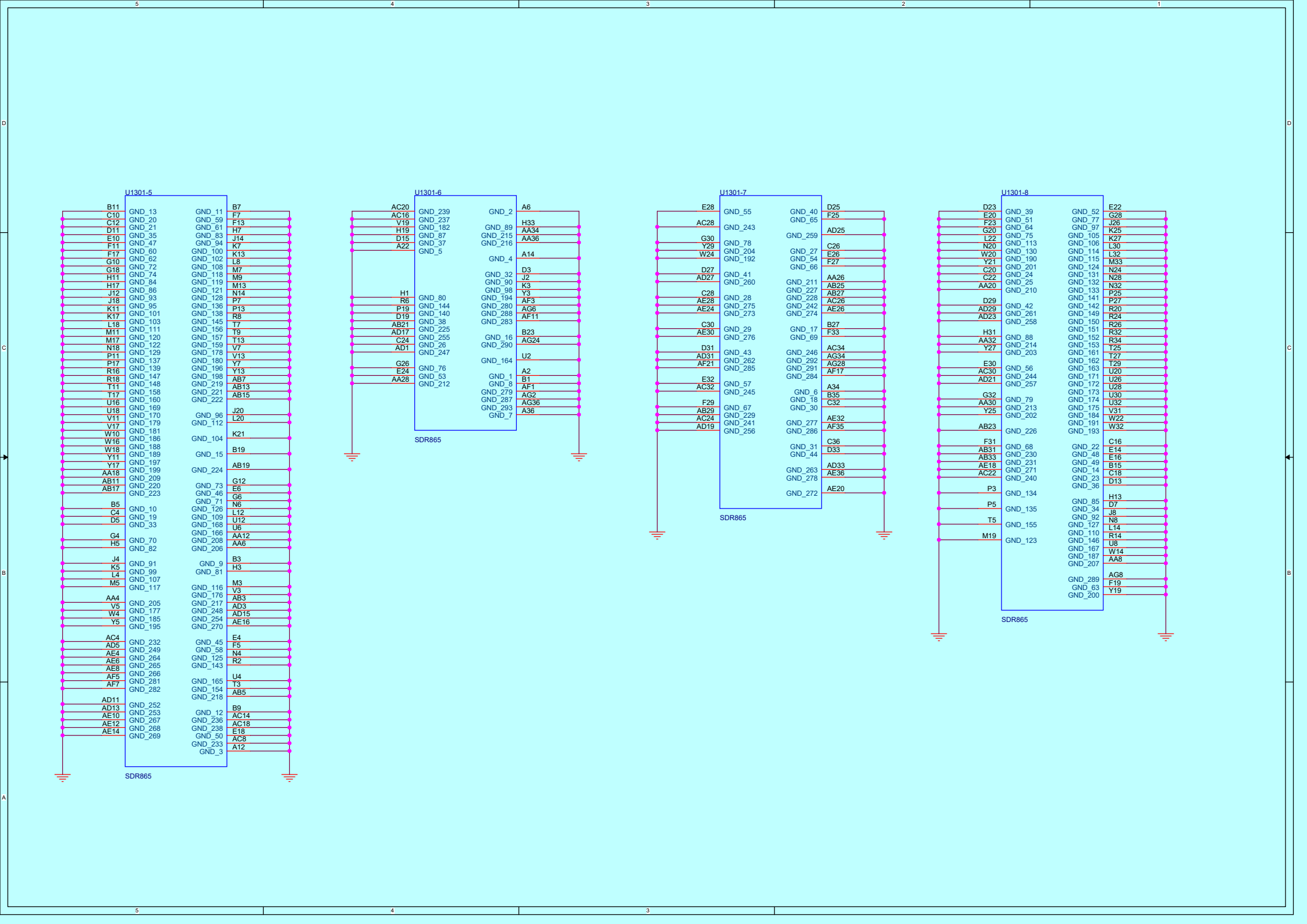


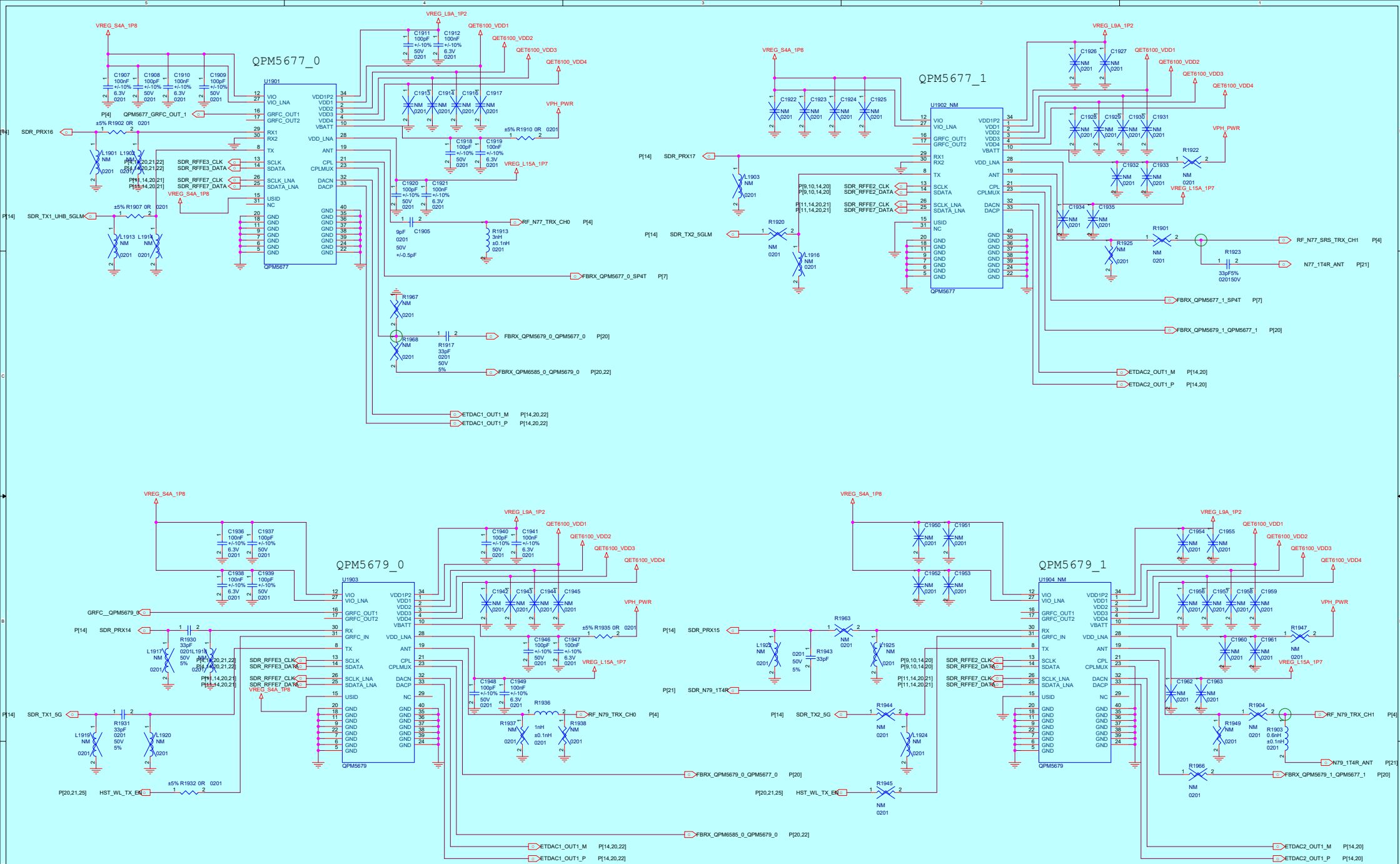


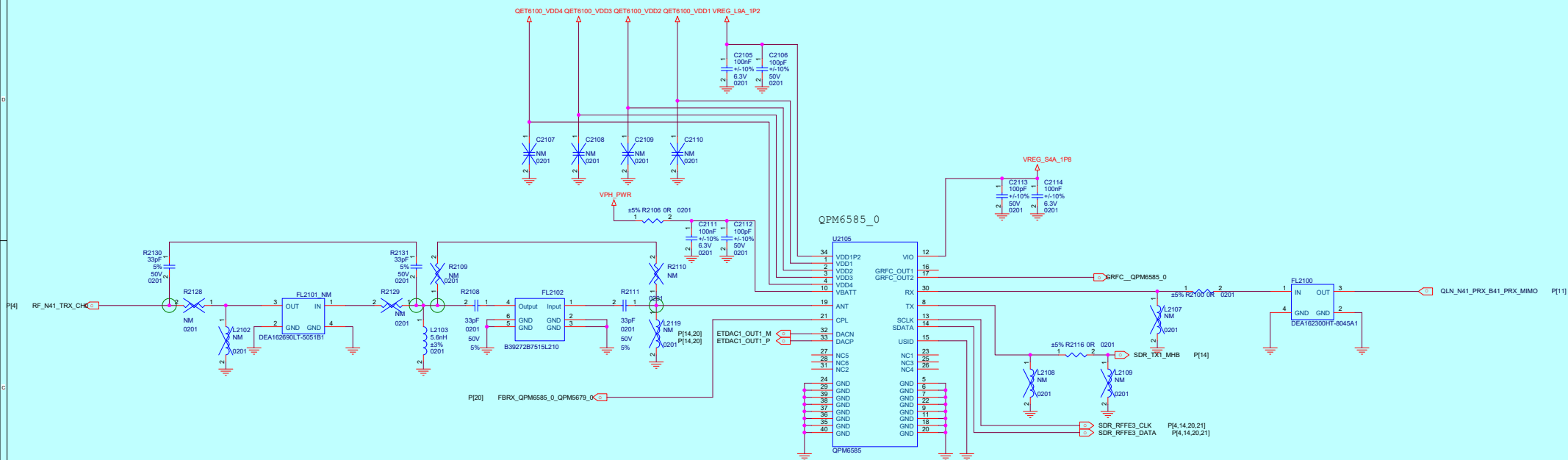


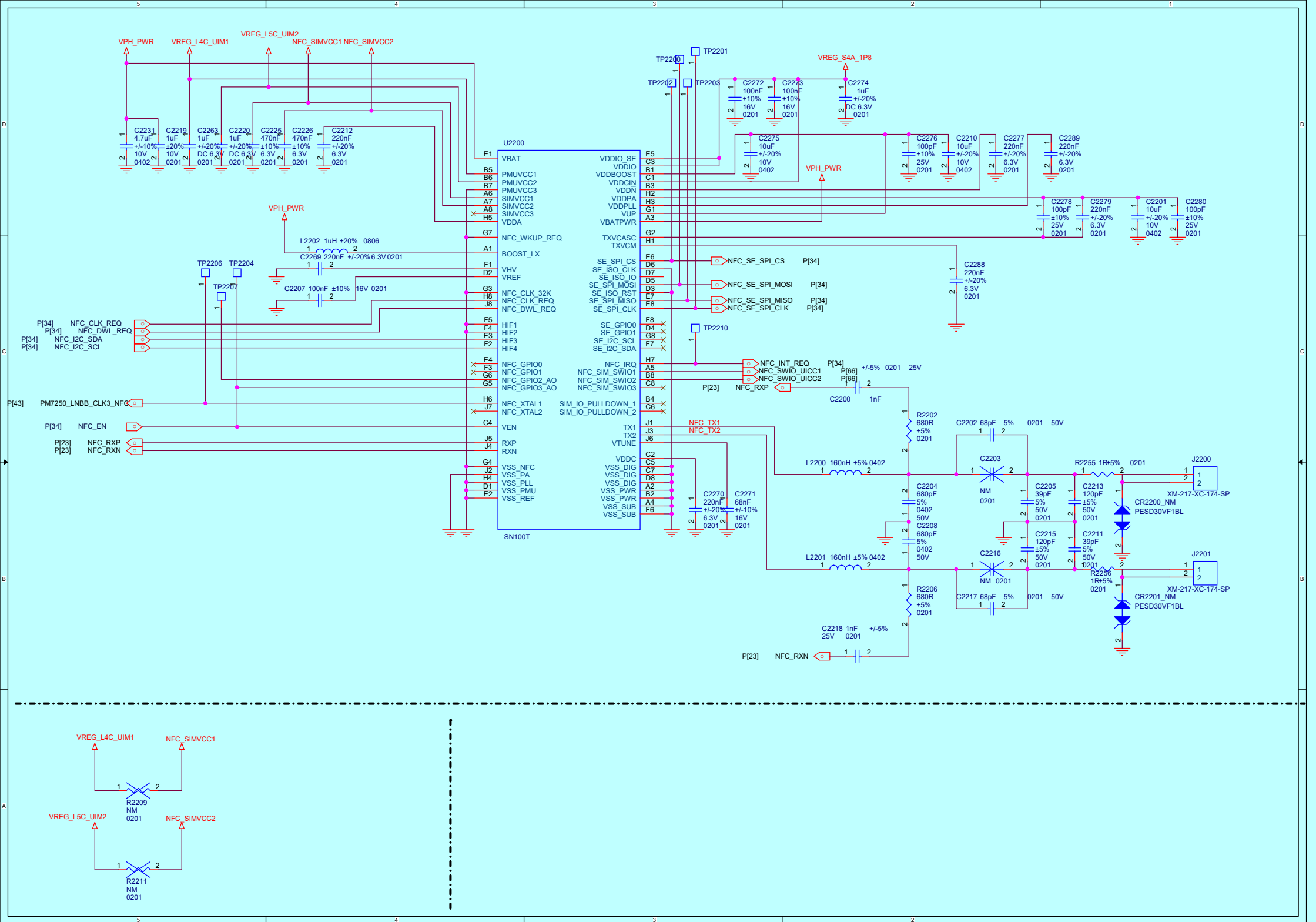


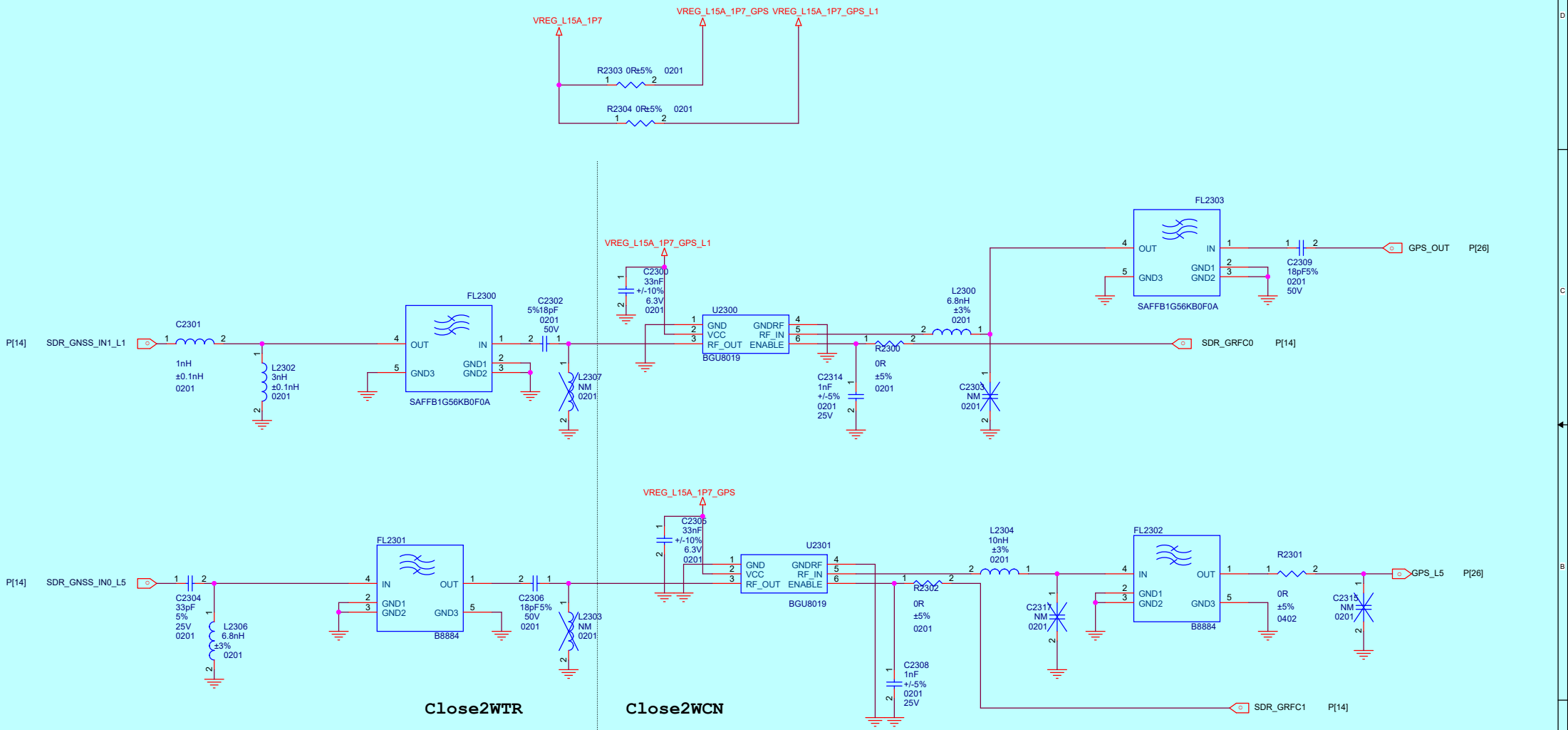


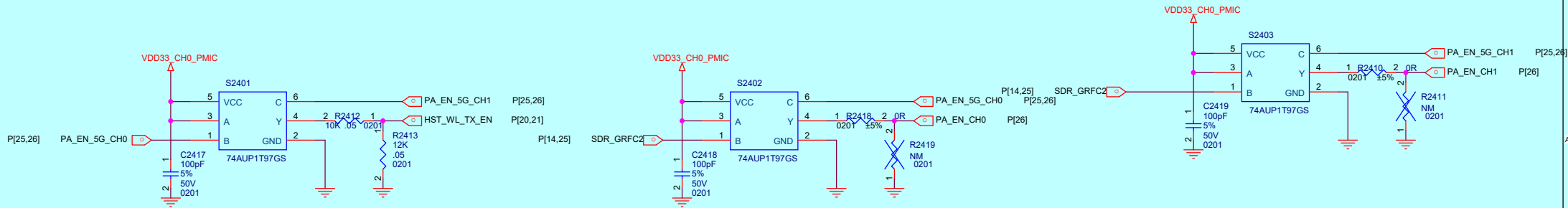
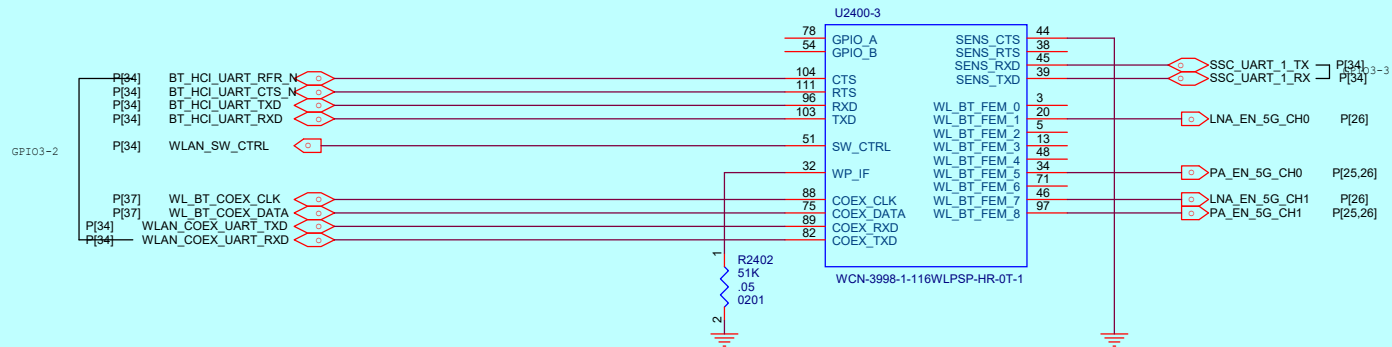
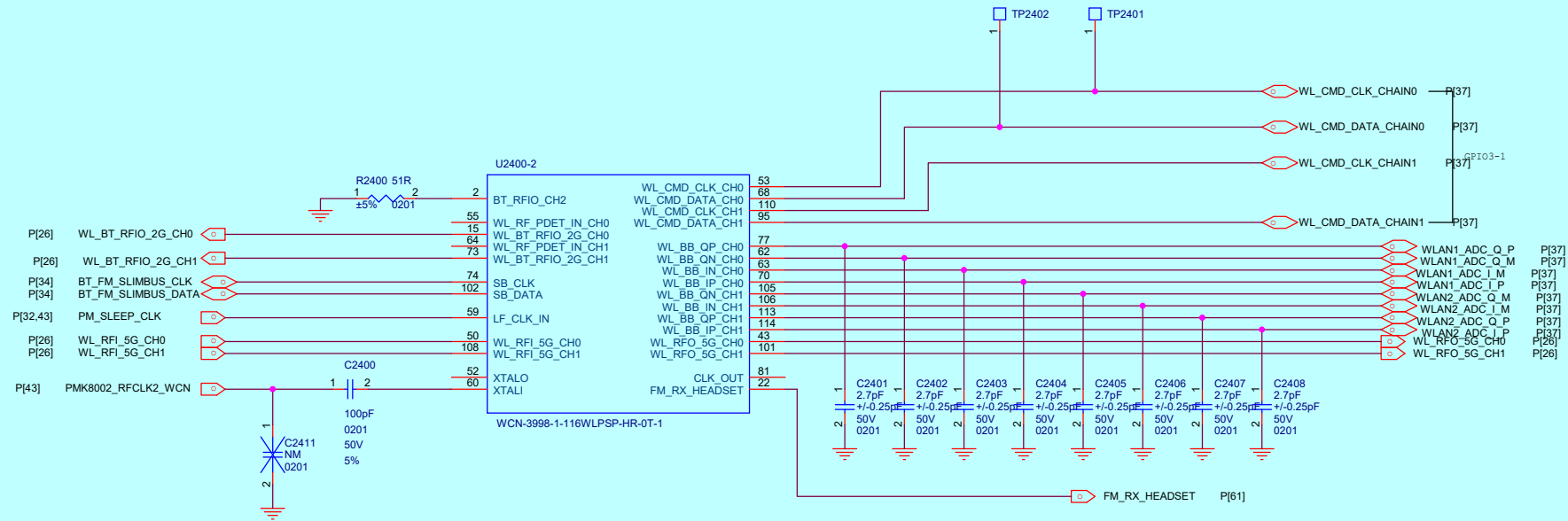


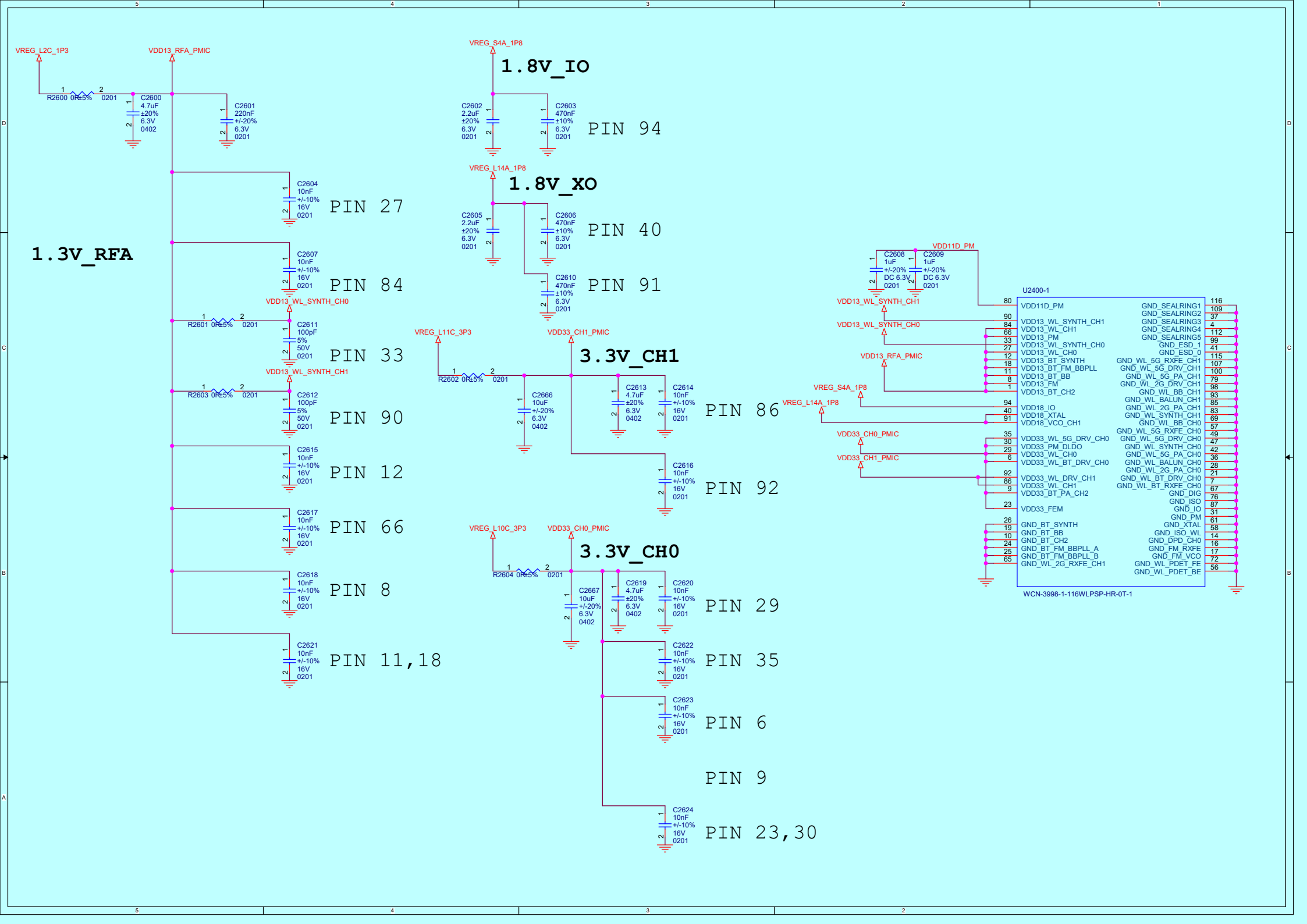


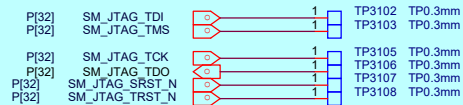
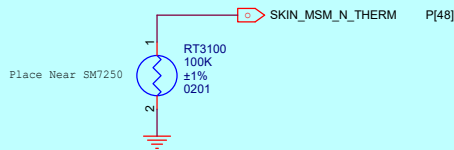
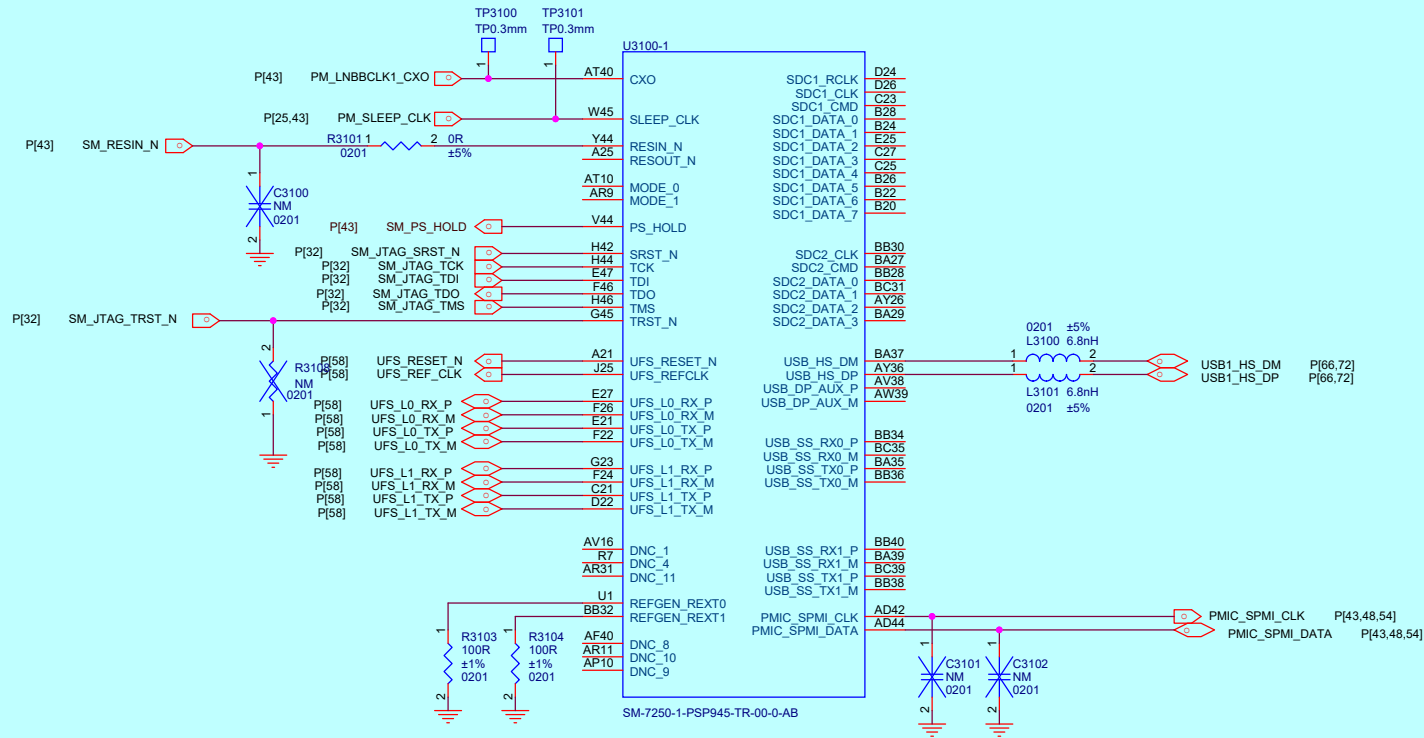


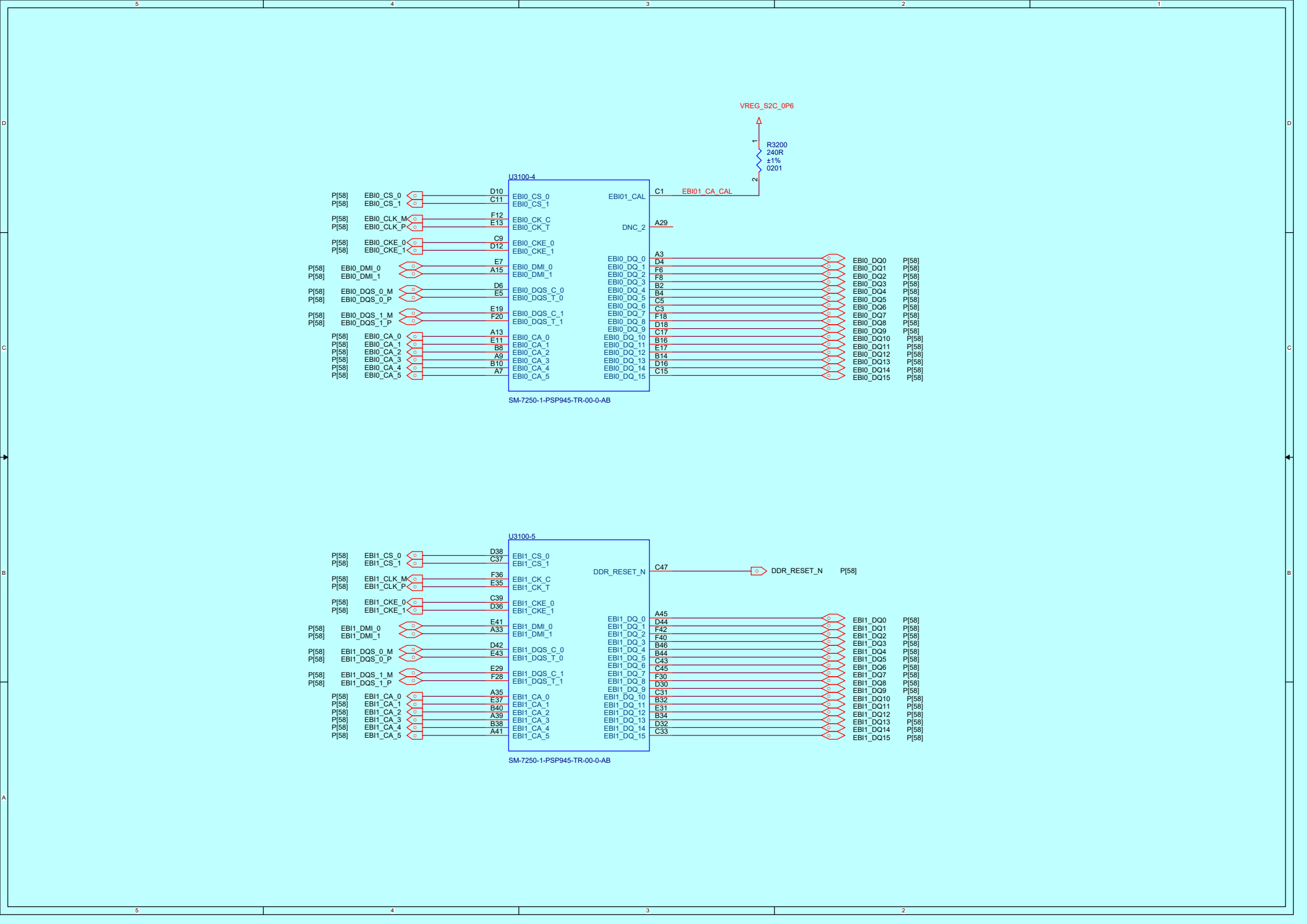












R3304
2.7K
±5%
0201



Note: By default `FORCE_USB_POL_SEL` state is low

The figure contains three schematic diagrams of the VREG_S4A_1P8 voltage regulator circuit, each showing a different load condition. Each circuit includes a 2.2K resistor (R330), a 0.05 capacitor (C020), and a 0.02 capacitor (C021).

- TS Load (Top):** The load is represented by a TS_ICC_SDA and TS_ICC_SCL. The input is labeled P[34.65] and the output is labeled TS_ICC_SDA.
- SPKR Load (Bottom Left):** The load is represented by a SPKR_ICC_SDA and SPKR_ICC_SCL. The input is labeled P[34.61] and the output is labeled SPKR_ICC_SDA.
- NFC Load (Bottom Right):** The load is represented by an NFC_ICC_SDA and NFC_ICC_SCL. The input is labeled P[23.34] and the output is labeled NFC_ICC_SDA.

SPK I2C1

Top Diagram (SCL):

- Resistor: R3301, 2.2K, 0.05, 0201
- Capacitor: 0.001uF
- Labels: P[34.65], P[34.66], TS, I2C, SDA, TS, I2C, SCL

Bottom Diagram (SDA):

- Resistor: R3330, 2.2K, 0.05, 0201
- Capacitor: 0.001uF
- Labels: P[34.61], P[34.61], SPKR, I2C, SDA, SPKR, I2C, SDA

TELE CAMERA

P[67] MIPI_DEPTH_TELE_CLK_P
P[67] MIPI_DEPTH_TELE_CLK_M
P[67] MIPI_DEPTH_TELE_LANE0_P
P[67] MIPI_DEPTH_TELE_LANE0_M
P[67] MIPI_TELE_LANE1_P
P[67] MIPI_TELE_LANE1_M

AC1
AD2
AD4
AE3
AF2
AG1
AG3
AH2
AH4
AJ3
CSI0_NC_CLK_P
CSI0_A0_CLK_M
CSI0_B0_LN0_P
CSI0_C0_LN0_M
CSI0_A1_LN1_P
CSI0_B1_LN1_M
CSI0_C1_LN2_P
CSI0_A2_LN2_M
CSI0_B2_LN3_P
CSI0_C2_LN3_M

U3100-6

CSI2_NC_CLK_P
CSI2_A0_CLK_M
CSI2_B0_LN0_P
CSI2_C0_LN0_M
CSI2_A1_LN1_P
CSI2_B1_LN1_M
CSI2_C1_LN2_P
CSI2_A2_LN2_M
CSI2_B2_LN3_P
CSI2_C2_LN3_M

CSI3_NC_CLK_P
CSI3_A0_CLK_M
CSI3_B0_LN0_P
CSI3_C0_LN0_M
CSI3_A1_LN1_P
CSI3_B1_LN1_M
CSI3_C1_LN2_P
CSI3_A2_LN2_M
CSI3_B2_LN3_P
CSI3_C2_LN3_M

AC3
AB2
AA3
Y4
Y2
W3
W1
V2
U3
T2
MIPI_W_CLK_P
MIPI_W_CLK_M
MIPI_W_LANE0_P
MIPI_W_LANE0_M
MIPI_W_LANE1_P
MIPI_W_LANE1_M
MIPI_W_LANE2_P
MIPI_W_LANE2_M
MIPI_W_LANE3_P
MIPI_W_LANE3_M

P42
N41
T42
R41
T44
R43
N43
M44
M42
L43
DSI1_B1_CLK_P
DSI1_C1_CLK_M
DSI1_A0_LN0_P
DSI1_B0_LN0_M
DSI1_C0_LN1_P
DSI1_A1_LN1_M
DSI1_A2_LN2_P
DSI1_B2_LN2_M
DSI1_C2_LN3_P
DSI1_NC_LN3_M

ULTRA CAMERA

P[70]
P[70]
P[70]
P[70]
P[70]
P[70]
P[67]
P[67]
P[67]

MICRO CAMERA

WIDE CAMERA

P[68]
P[68]
P[68]
P[68]
P[68]
P[68]
P[68]
P[68]
P[68]
P[68]

Front 44M CAMERA

P[69] MIPI_F_CLK_P
P[69] MIPI_F_CLK_M
P[69] MIPI_F_LANE0_P
P[69] MIPI_F_LANE0_M
P[69] MIPI_F_LANE1_P
P[69] MIPI_F_LANE1_M
P[69] MIPI_F_LANE2_P
P[69] MIPI_F_LANE2_M
P[69] MIPI_F_LANE3_P
P[69] MIPI_F_LANE3_M

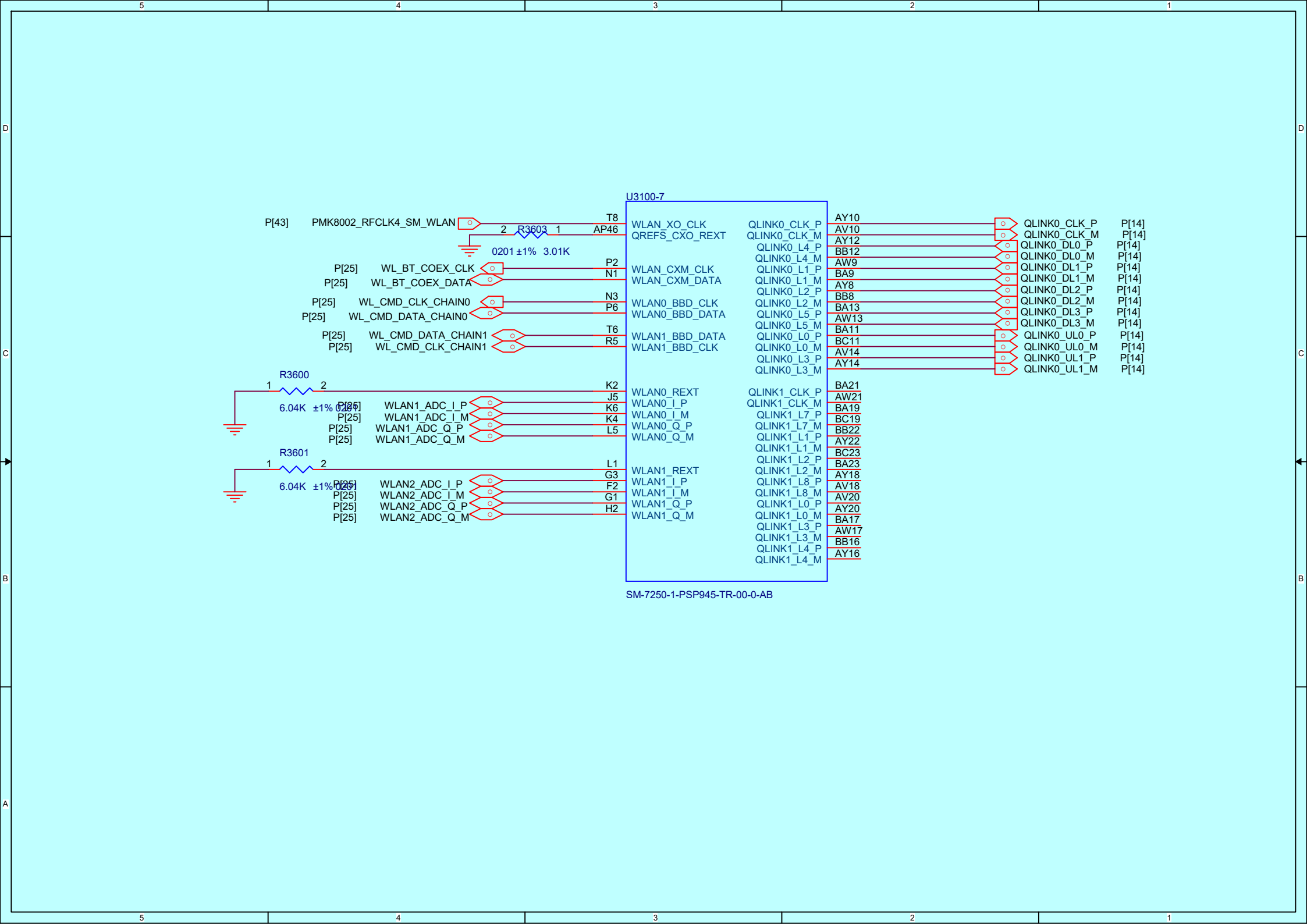
AD6
AE7
AE5
AF4
AF6
AG5
AG7
AH6
AH8
AJ7
CSI1_NC_CLK_P
CSI1_A0_CLK_M
CSI1_B0_LN0_P
CSI1_C0_LN0_M
CSI1_A1_LN1_P
CSI1_B1_LN1_M
CSI1_C1_LN2_P
CSI1_A2_LN2_M
CSI1_B2_LN3_P
CSI1_C2_LN3_M

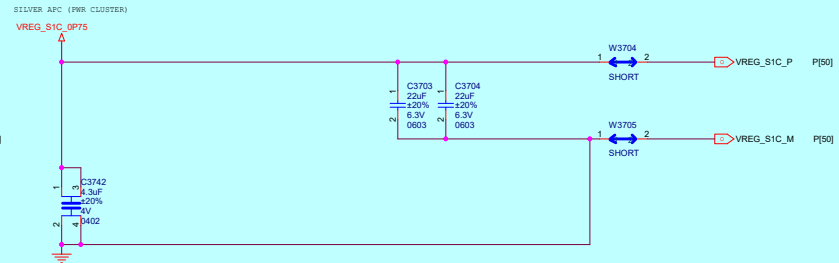
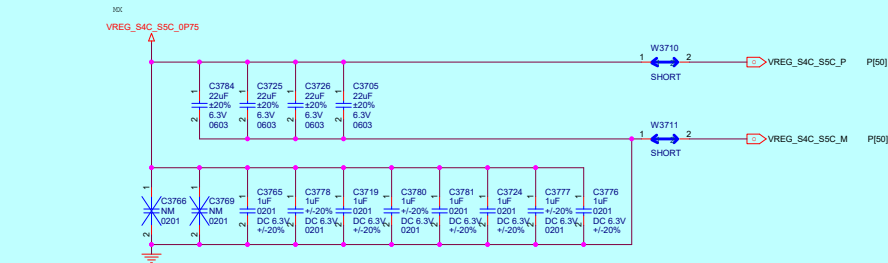
P[65] MIPI_DSIO_CLK_P
P[65] MIPI_DSIO_CLK_M
P[65] MIPI_DSIO_LANE0_P
P[65] MIPI_DSIO_LANE0_M
P[65] MIPI_DSIO_LANE1_P
P[65] MIPI_DSIO_LANE1_M
P[65] MIPI_DSIO_LANE2_P
P[65] MIPI_DSIO_LANE2_M
P[65] MIPI_DSIO_LANE3_P
P[65] MIPI_DSIO_LANE3_M

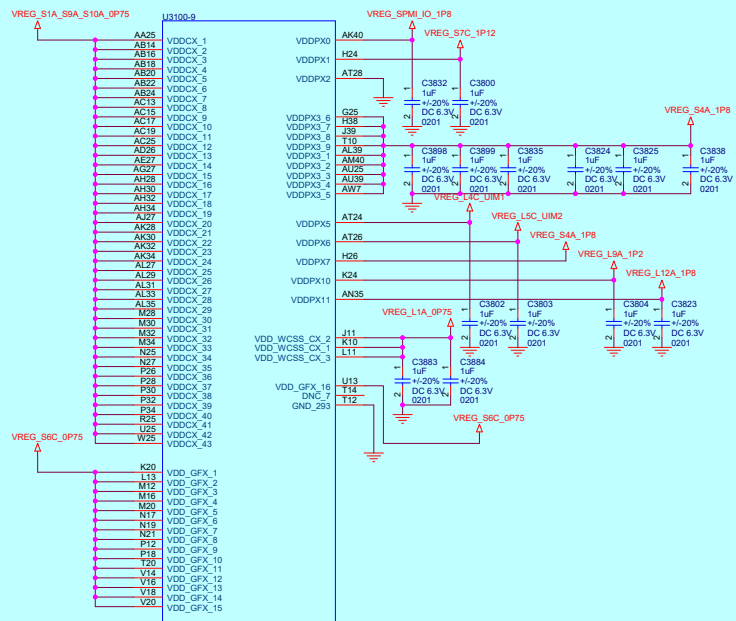
R45
P44
N47
M46
P46
N45
U45
T46
V46
U47
DSIO_B1_CLK_P
DSIO_C1_CLK_M
DSIO_A0_LN0_P
DSIO_B0_LN0_M
DSIO_C0_LN1_P
DSIO_A1_LN1_M
DSIO_A2_LN2_P
DSIO_B2_LN2_M
DSIO_C2_LN3_P
DSIO_NC_LN3_M

SM-7250-1-PSP945-TR-00-0-AB

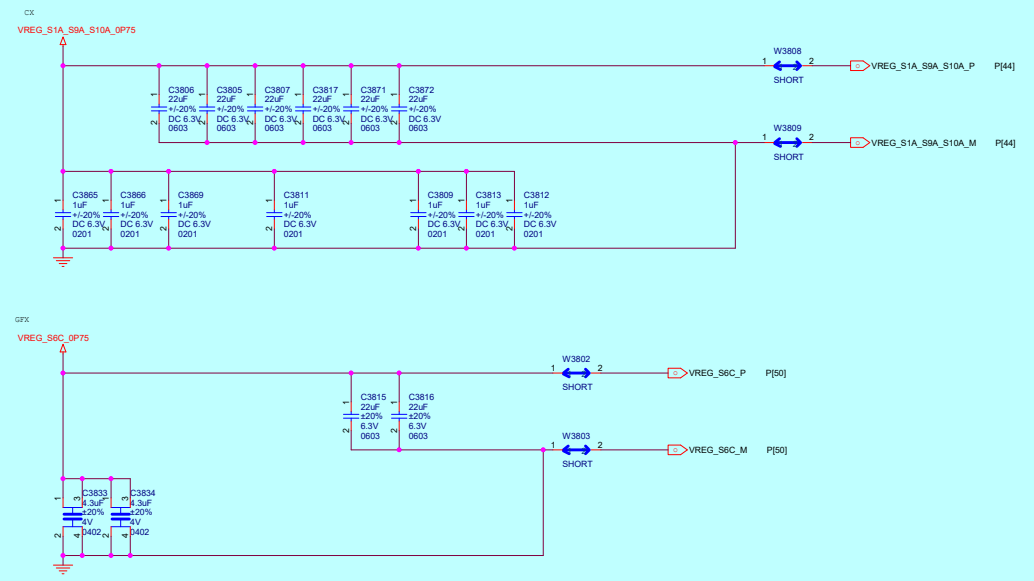
MIPI SWITCH

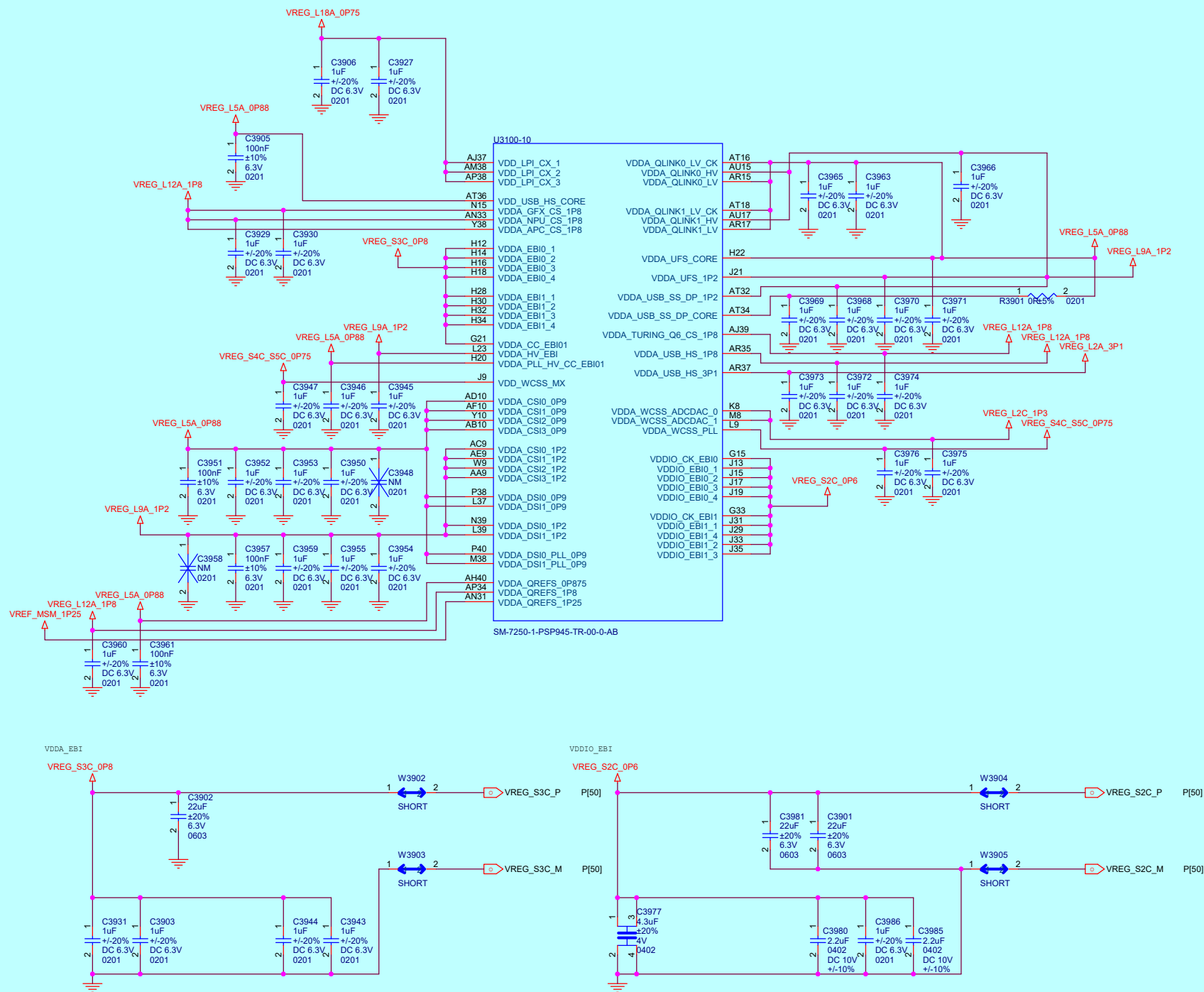


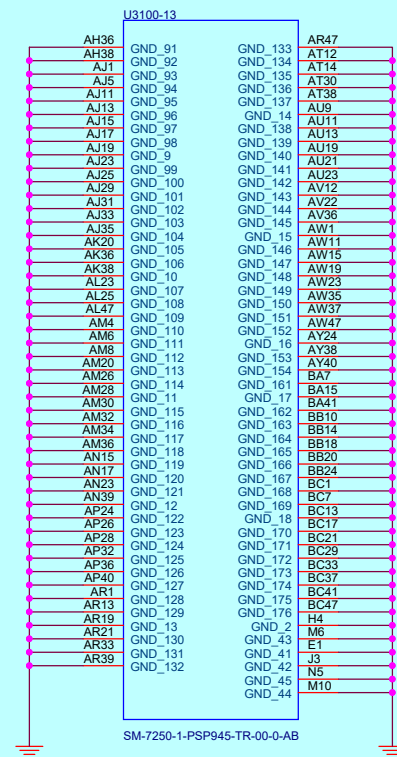
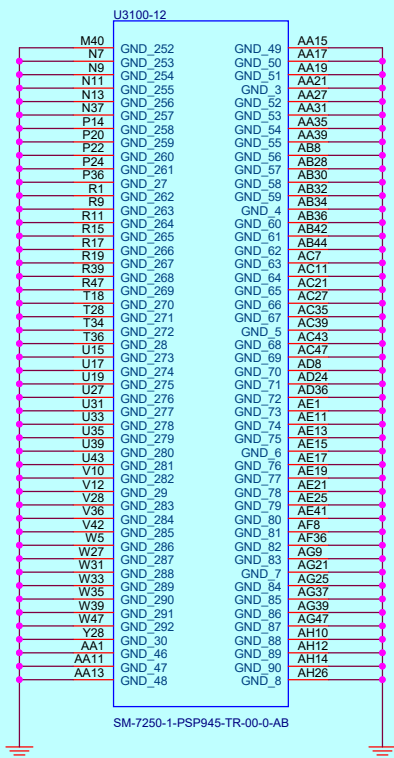
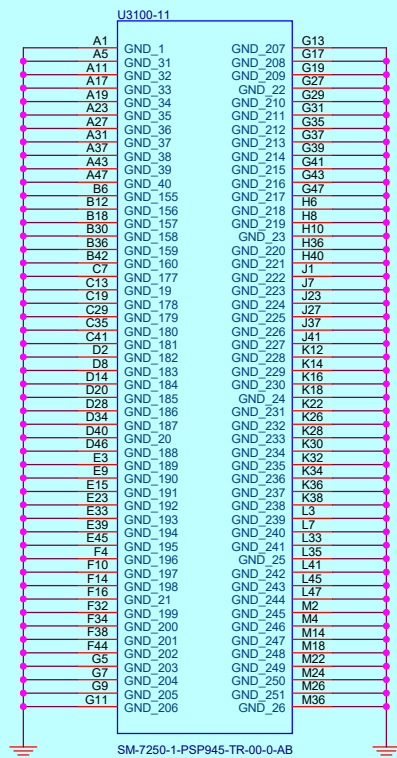
[illegible]

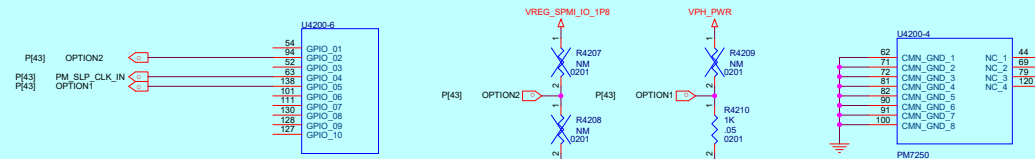


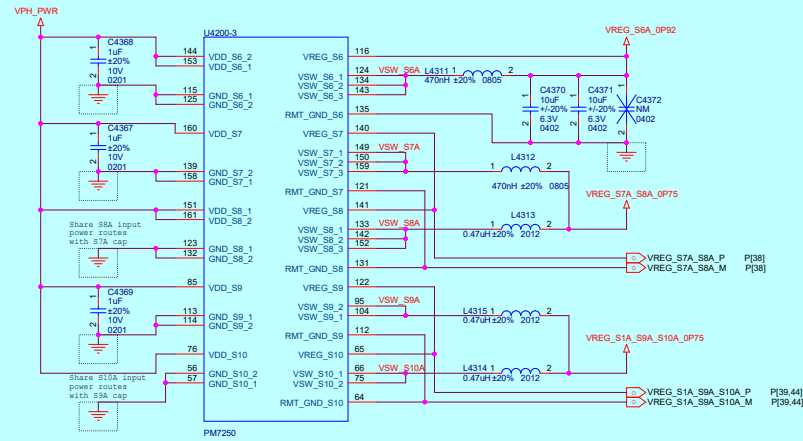
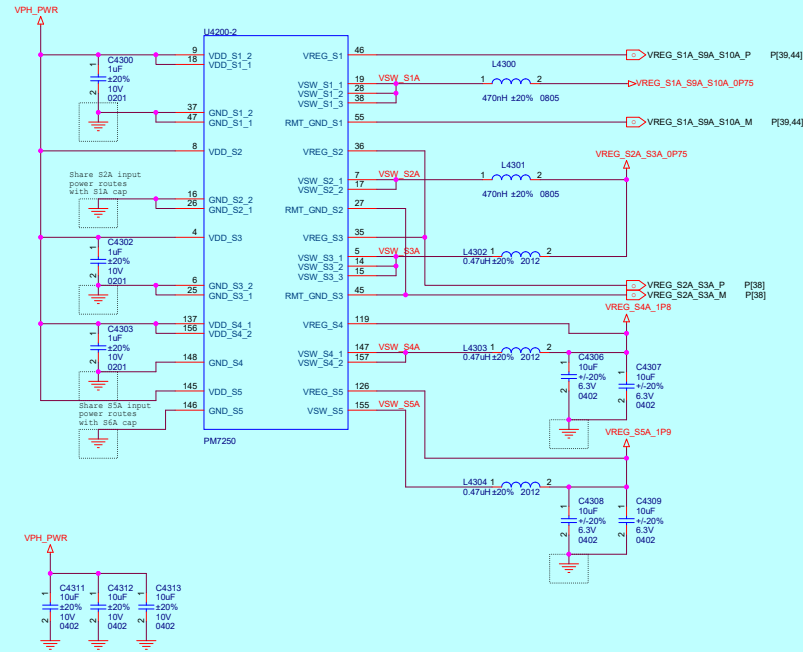
SM-7250-1-PS-P945-TR-00-0-AB

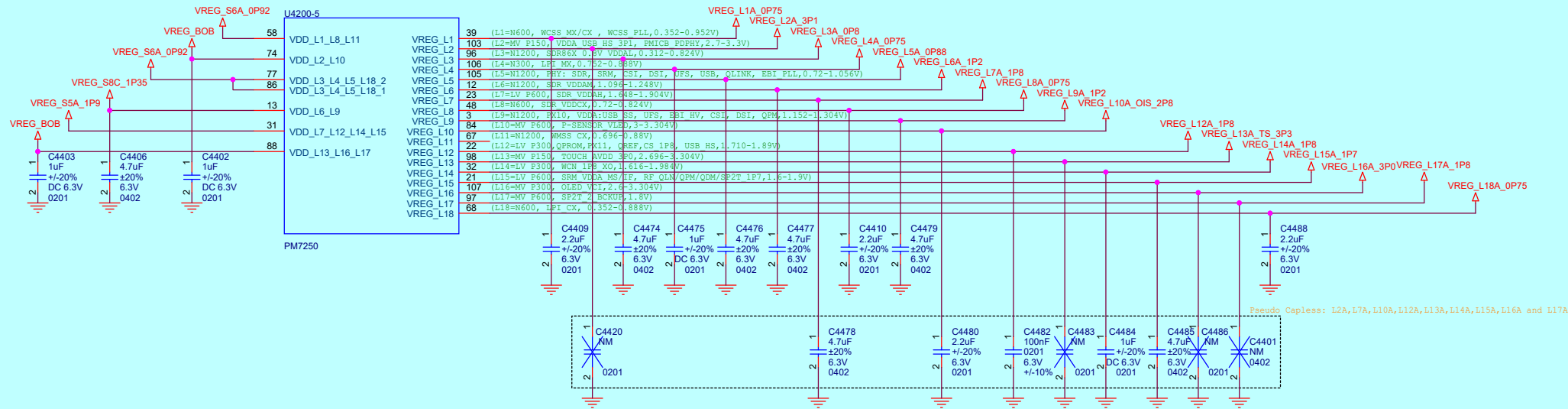






[illegible]

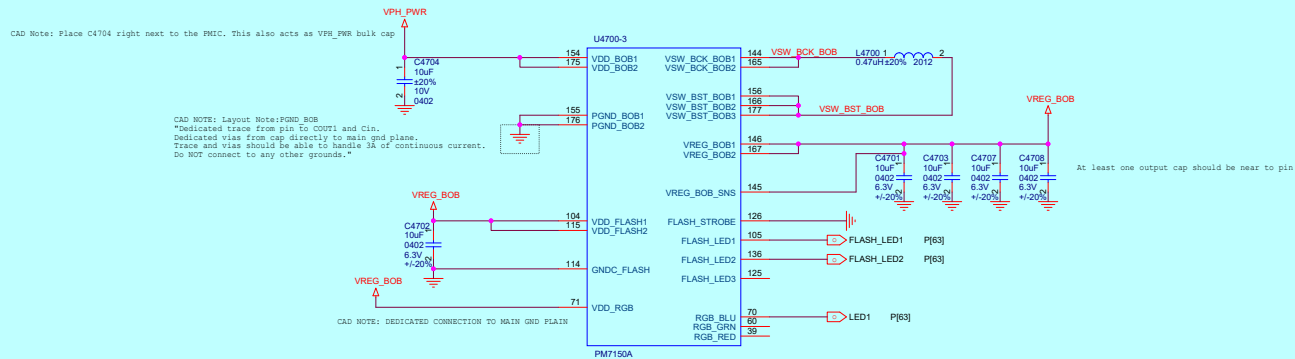


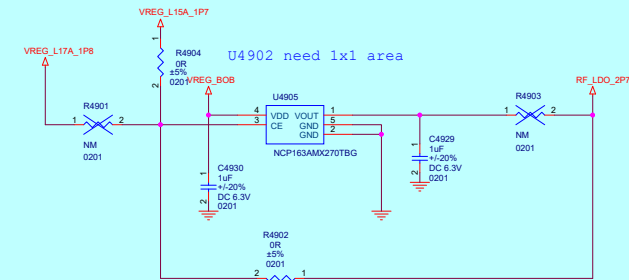
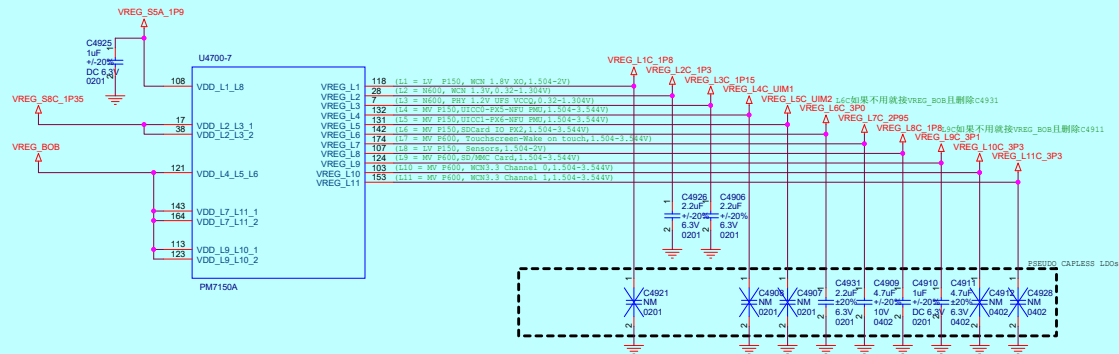
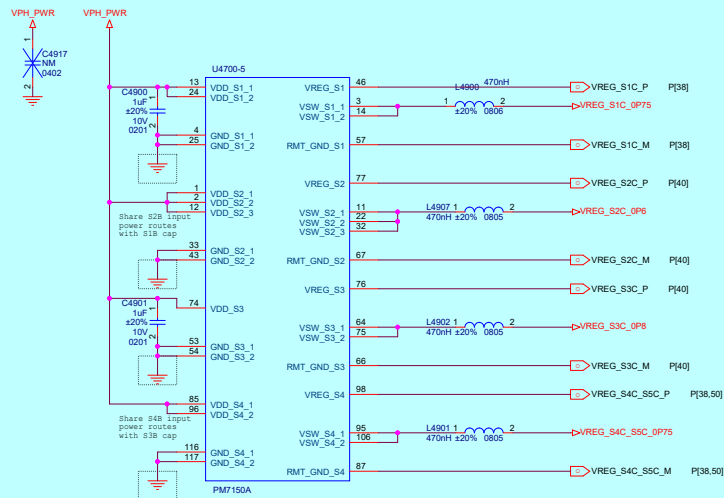


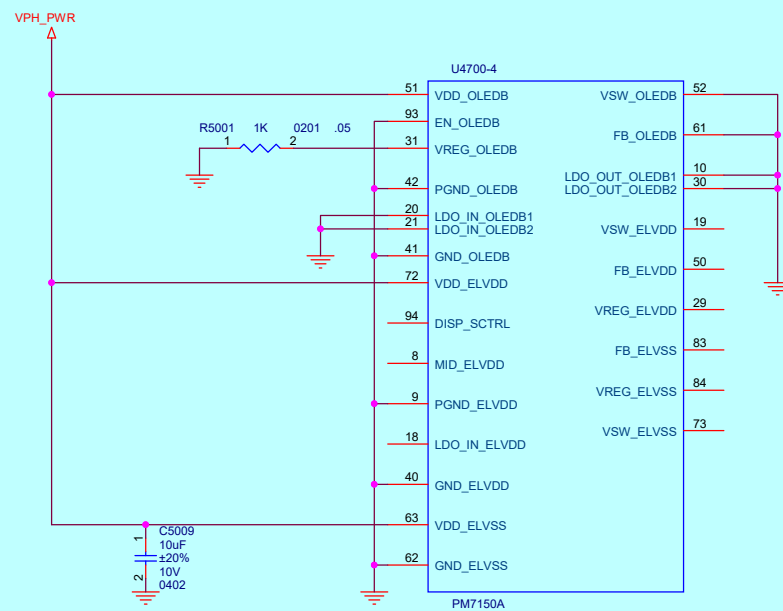
NOTE: PMIC internal regulators used VREG_L12A : BBCLK_DRV

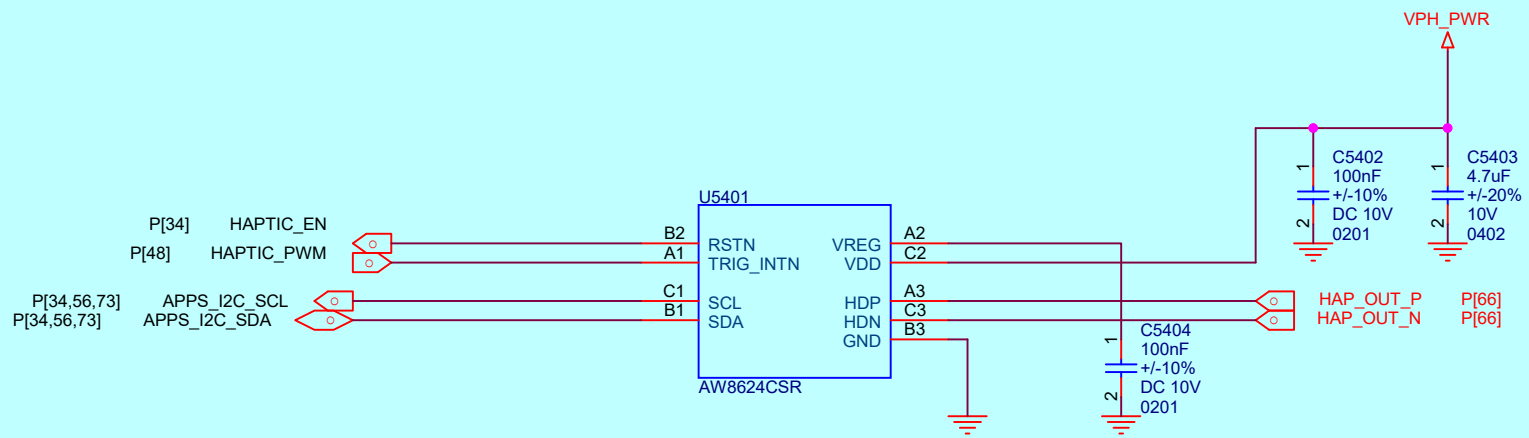
NOTE: P-type LDOs are pseudo-capless, capacitors can be placed near load. Regulators powering PMIC internal circuits need capacitors near PMIC. N-type LDOs with >300mA rating need local capacitors near PMIC.

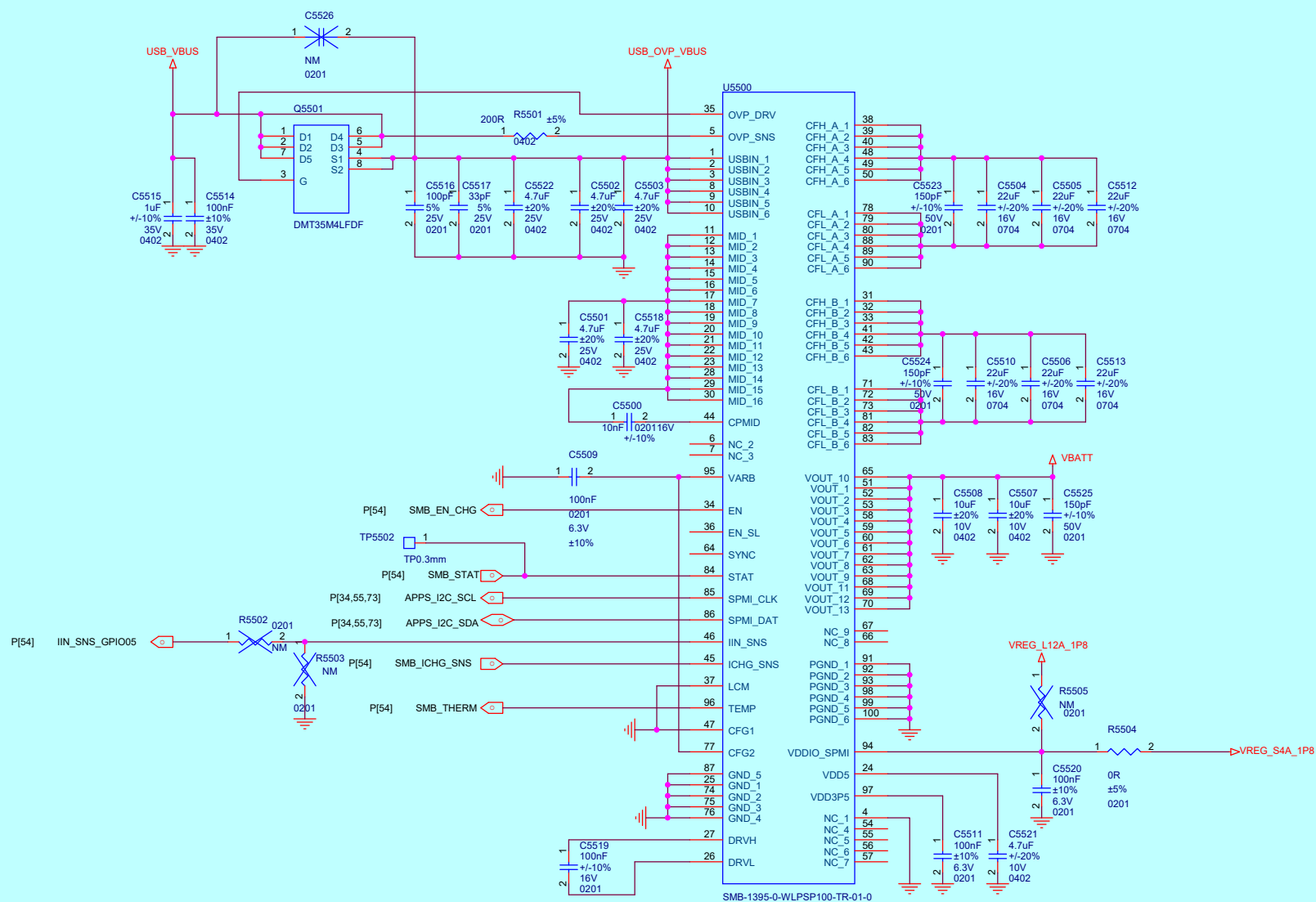
PM7150A_BOB/FLASH

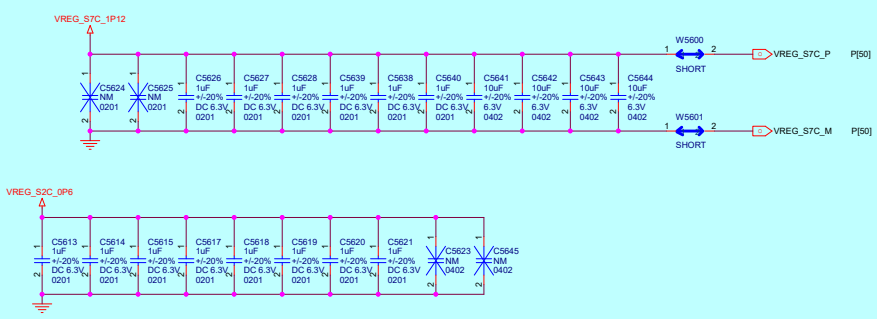
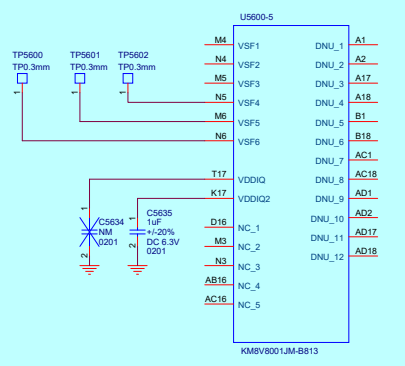
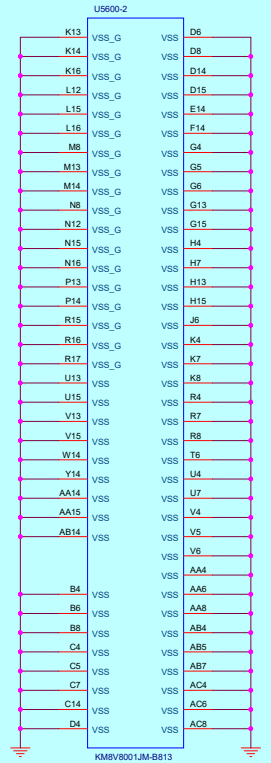
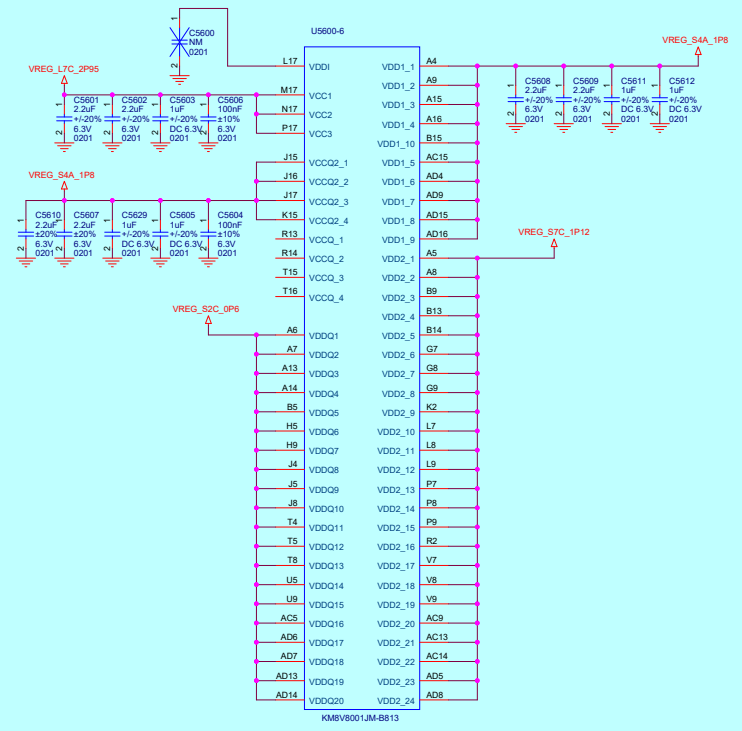




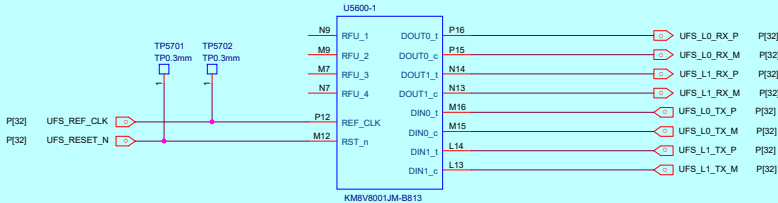




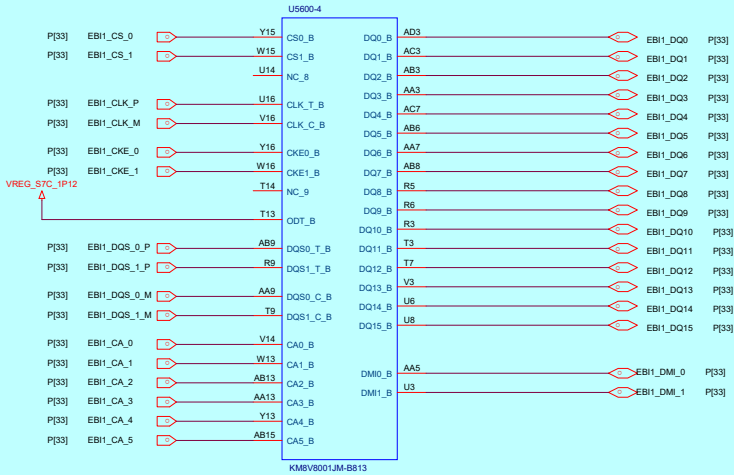
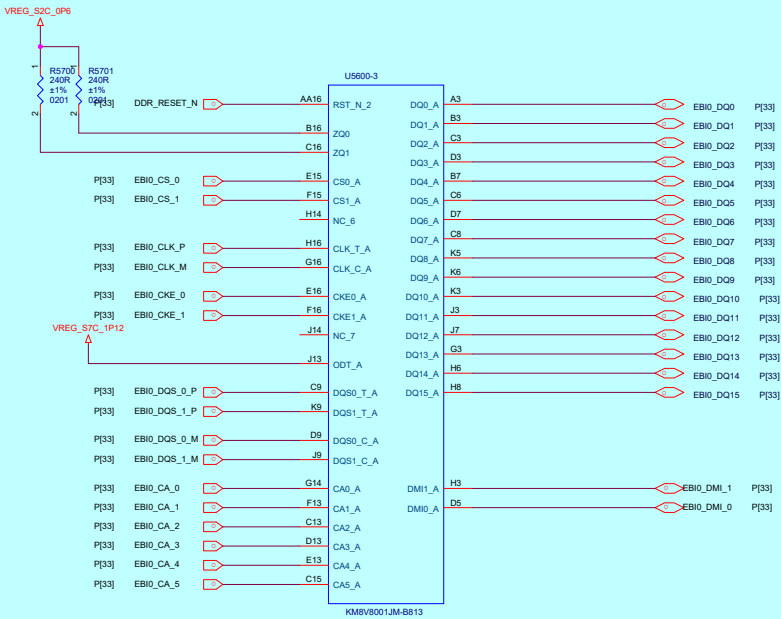


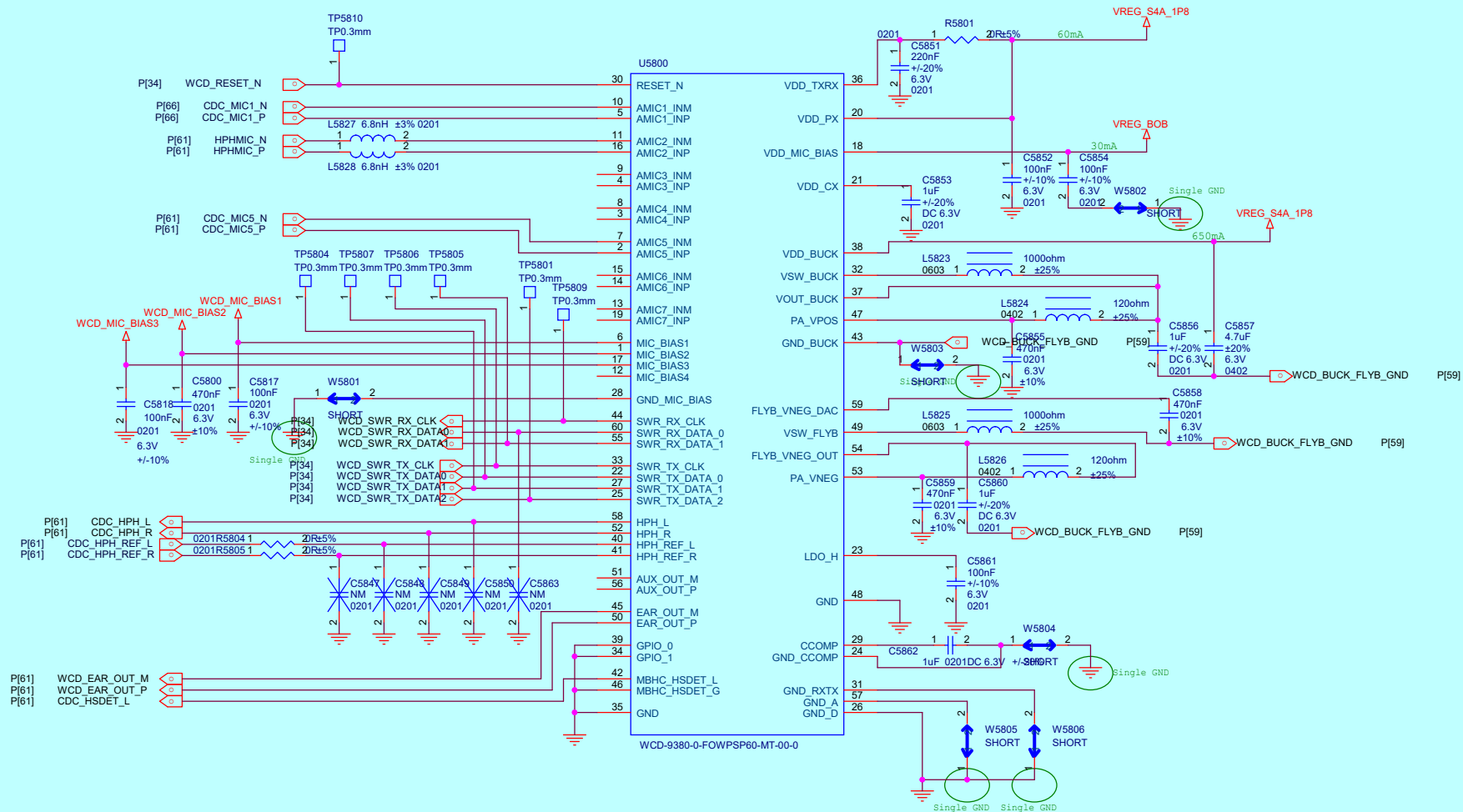


UFS 2.1

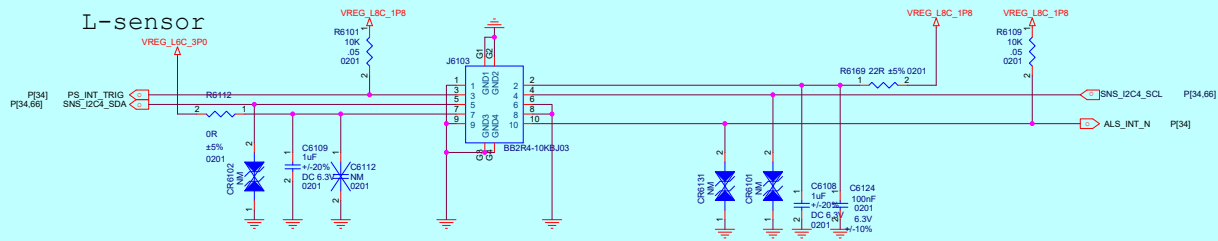


LPDDR4 / 4x

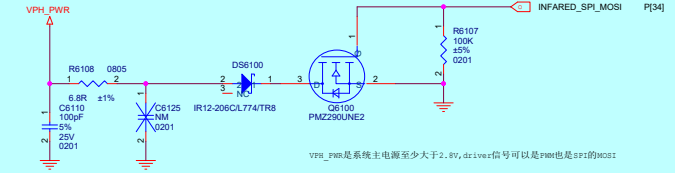




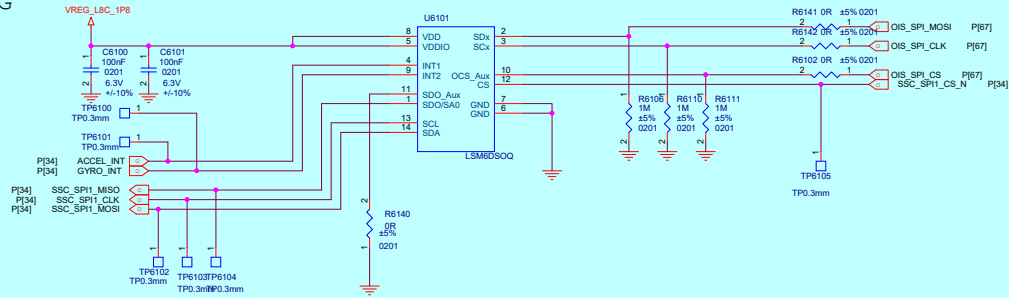
L-sensor



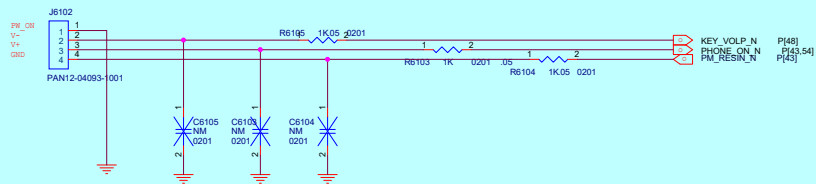
INFARED



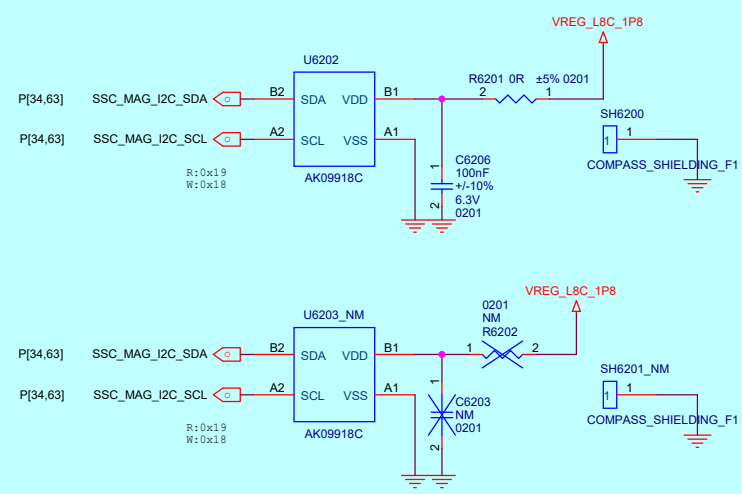
A+G



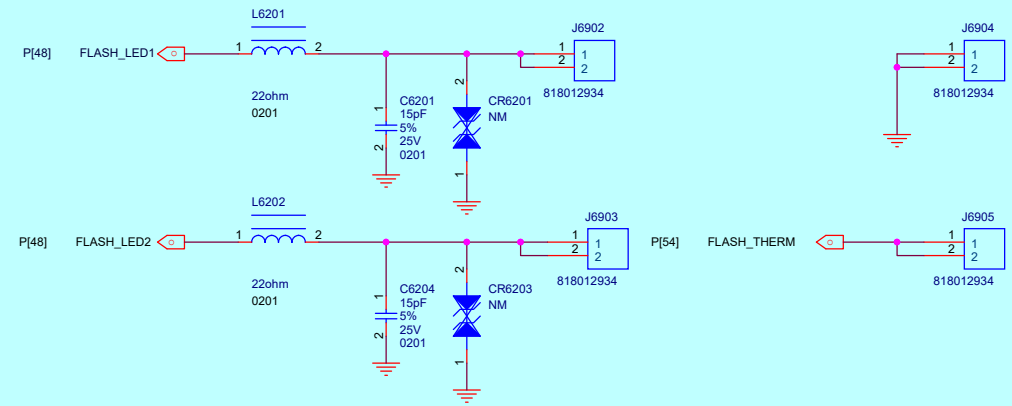
Sidekey



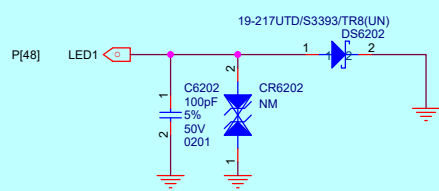
COMPASS

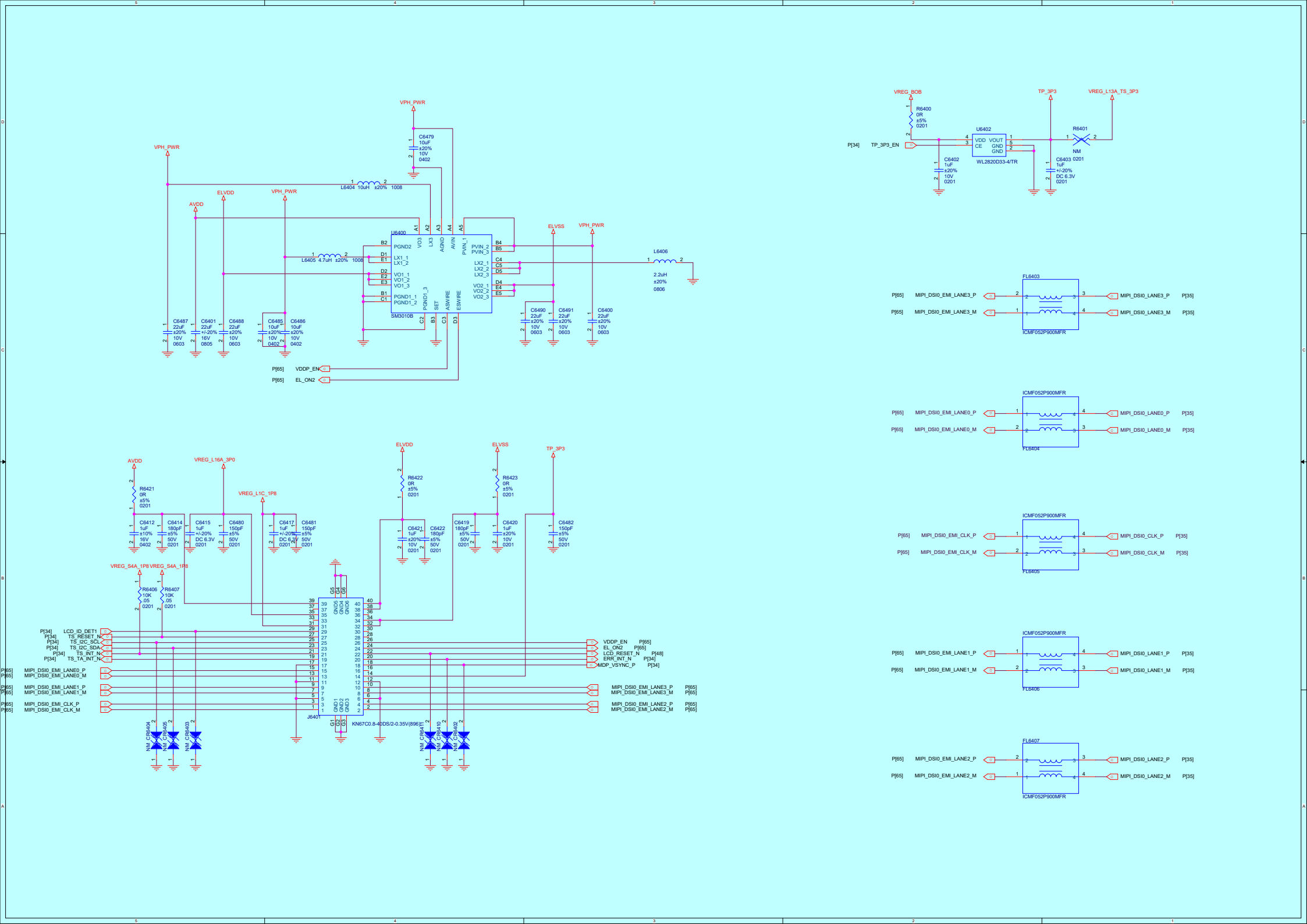


FLASH LED

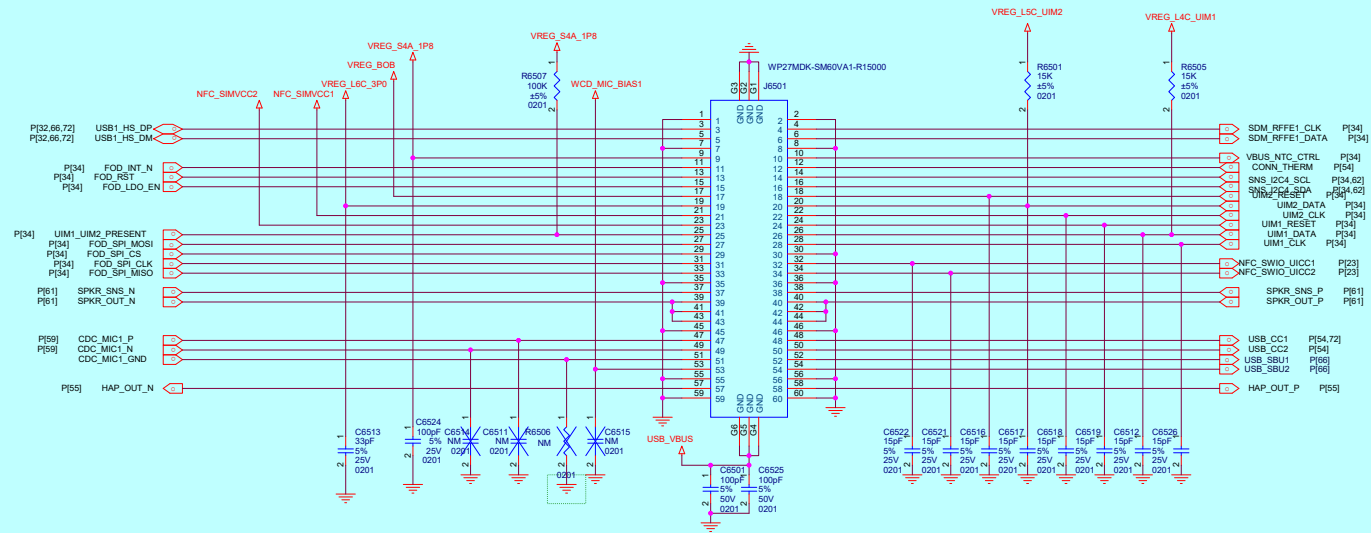


LED

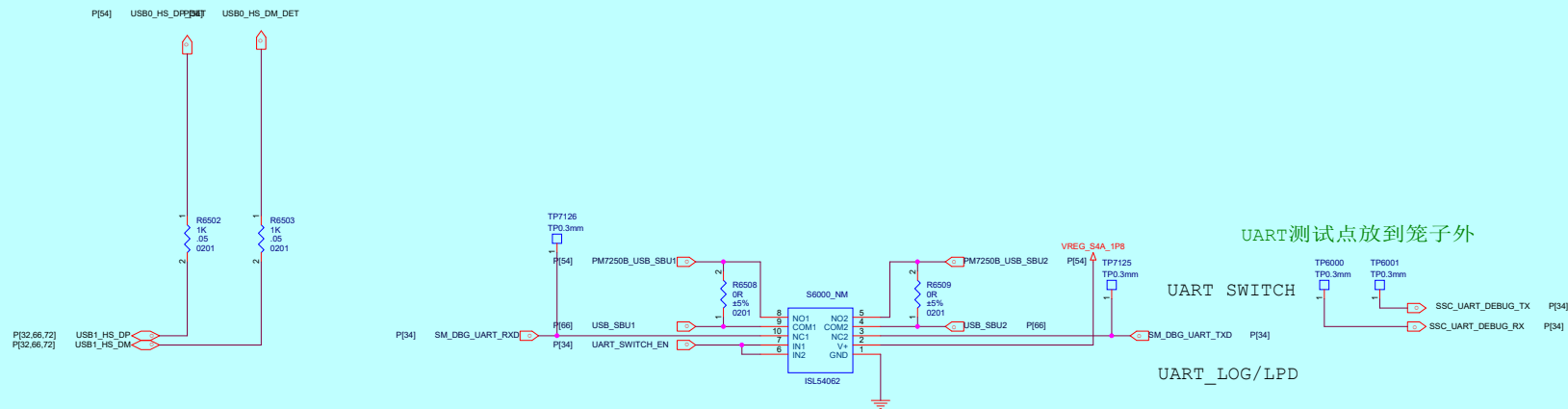


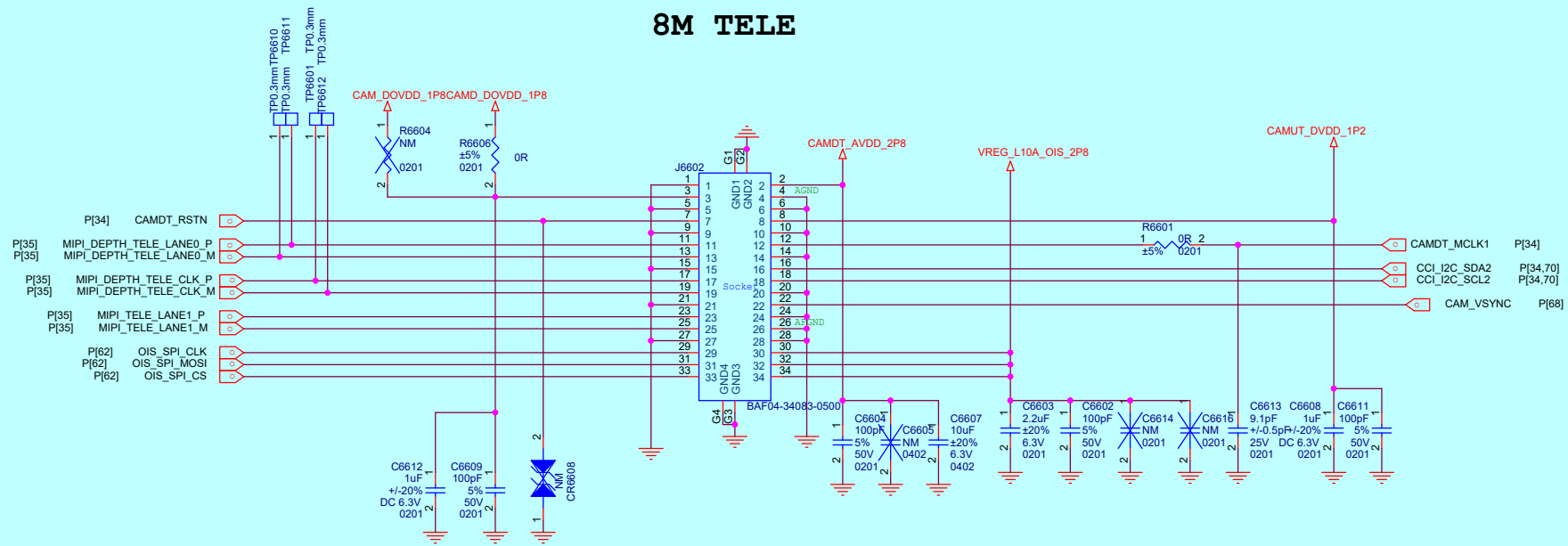
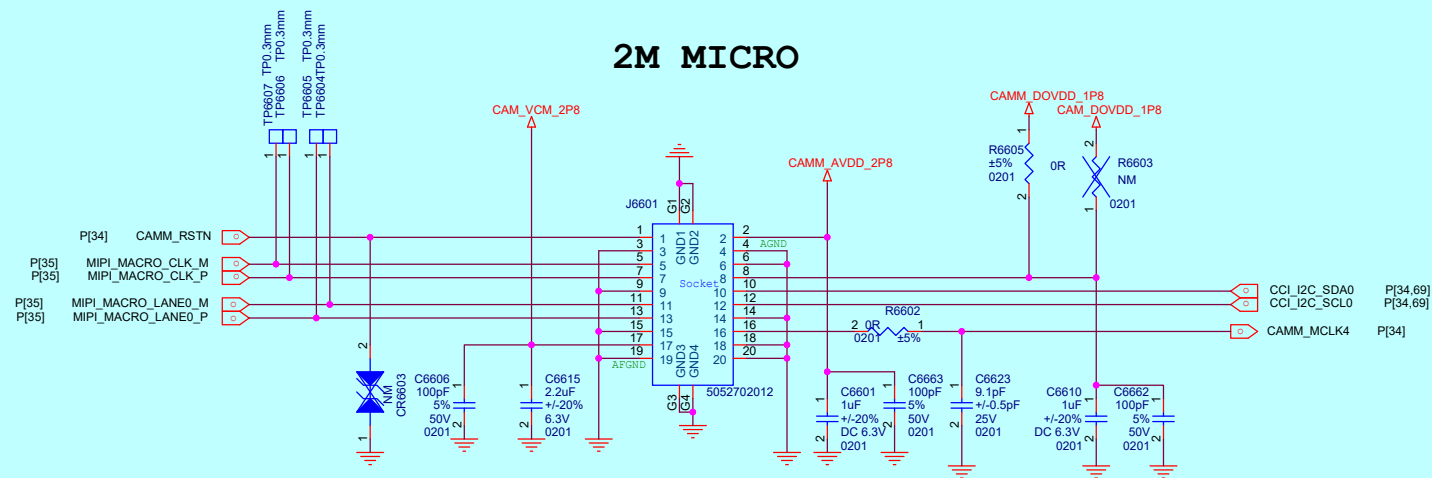


BTB CONNECTOR

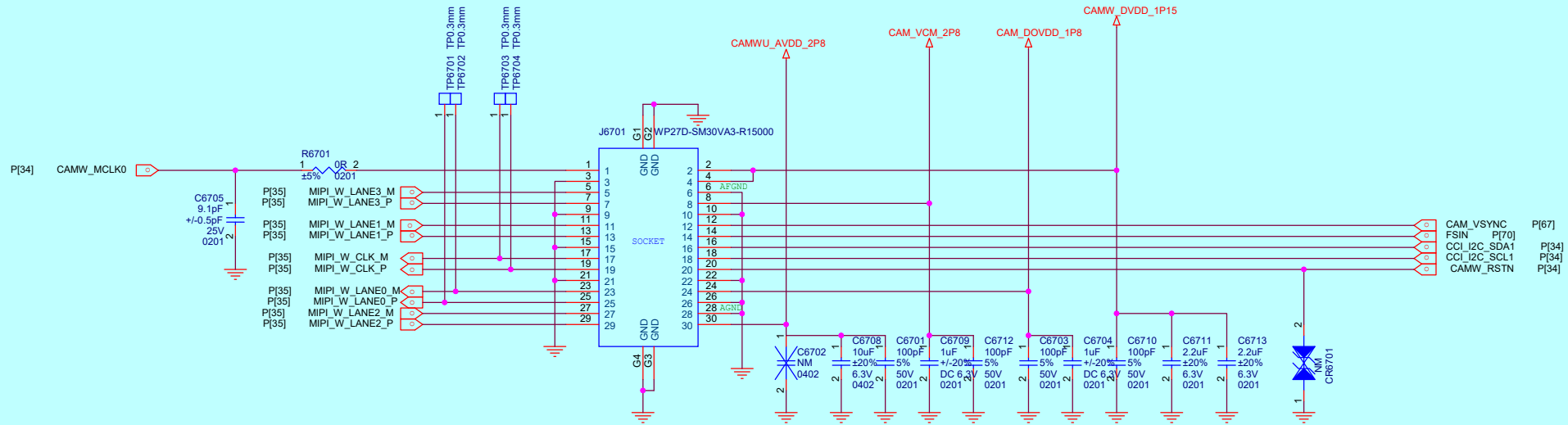


干净地方单独下主GND

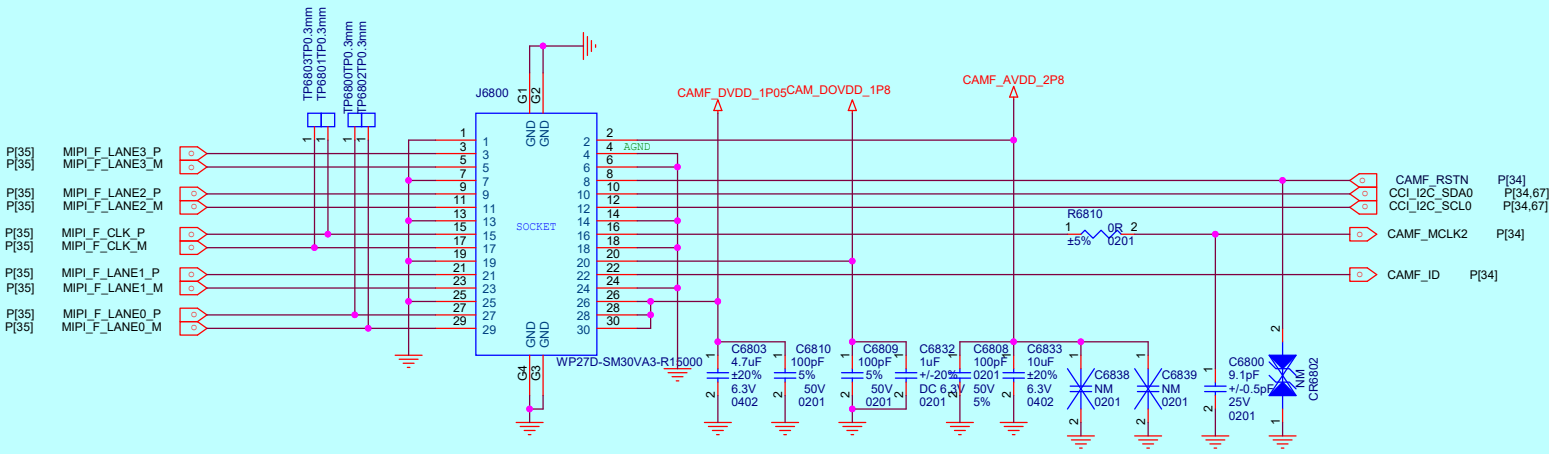




48M WIDE



44M FRONT



8M ULTRA

